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A Final Report for:

AN ACCELERATED PROGRAM FOR LOW-COST CdZnTe/GaAs/Si SUBSTRATES FOR MCT INFRARED FOCAL PLANE ARRAYS

Submitted under:
Contract No. MDA972-92-C-0039

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Defense Advanced Research Projects Agency
Microelectronics Technology Office (MTO)

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Nasser H. Karam, Ph.D.

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Spire Corporation
One Patriots Park
Bedford, MA 01730-2396

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13. ABSTRACT *(Maximum 200 words)*

The objective of this program was to develop CdZnTe/GaAs/Si alternative substrates by metalorganic chemical vapor deposition (MOCVD) for MCT liquid-phase epitaxy (LPE). The purpose was to make available larger, more robust, and far less expensive substrates than currently produced bulk CdZnTe, the substrates should be compatible with LPE and free of the limitation on detector array dimensions imposed by the thermal expansion mismatch between mercury-cadmium-telluride and bump-bonded silicon circuitry.

As a result at the substrate I program a thermal oxide encapsulant has been developed that is impervious to the Te-rich LPE melt and is not wetted by it. This encapsulant has made it possible to reduce the Ga impurity level in LPE HgCdTe to below 1 x 10^{15} atoms/cm^3. At the same time it has been found possible to produce CdZnTe deposits with a (111) B orientation that are free of twins at the surface and are of excellent crystalline quality with dislocation densities of down to 5 x 10^5/cm^2 and an X-ray rocking curve FWHM of below 80 arc.sec. Long-wave infrared diodes with a quantum efficiency of 50% (when illuminated through the uncoated Si substrate) have been produced form this material.

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TABLE OF CONTENTS

		Page
1	PROGRAM GOALS AND STRATEGY	1
2	RESULTS AND STATUS	3
	2.1 Encapsulation	3
	2.2 Wafer Bow	8
	2.3 The MOCVD Reactor	10
	2.4 The Reactor Model	11
	2.5 MOCVD Growth	16
	2.6 LPE Growth of HgCdTe	18
	2.7 Diode and Array Test Data	30

LIST OF FIGURES

		Page
1	Single layer SILOX encapsulation, silicon wafers (deposition temperature)	4
2	Single layer SILOX encapsulation, silicon wafers (film thickness)	4
3	Single layer nitride encapsulation, silicon wafers (deposition temperature)	5
4	Single layer nitride encapsulation, silicon wafers (film thickness)	5
5	Single layer thermal oxide encapsulation (deposition temperature)	6
6	Single layer thermal oxide encapsulation (film thickness)	6
7	Two layer encapsulation summary, silicon wafers	7
8	Variation of bow in Si for different encapsulants a) thick layers and b) thin layers	9
9	Spire SPI-MOCVD™ 3000G MOCVD reactor (all sensors input through A/D to control CPU)	10
10	SPI-MOCVD 3000 G reactor	11
11	Comparison of calculated and average experimental temperatures of the outer wall	12
12	Gas flow streamlines predicted for the reactor under conditions similar to those used in a CdTe deposition run	13
13	Comparison of calculated growth rates with experiments	13
14	Comparison of the experimental and predicted reactor wall temperatures.	14
15	A comparison of the predicted deposition rates	15
16	Predicted streamlines for the turbulent model of the reactor	15
17	Surface morphology for CdZnTe films deposited on GaAs and GaAs/Si substrates with different orientations	17
18	(a) XTEM of (111) CdTe on GaAs/Si Film using BF g = <220>; (b) cross-sectional TEM of {111} orientation CdTe film using BF g = <220> on GaAs/Si	19

LIST OF FIGURES (Concluded)

		Page
19	Thickness uniformity mapping for $Cd_{0.96}Zn_{0.04}Te$ on 100 mm GaAs substrates deposited in Spire's SPI-MOCVD 3000G reactor	20
20	Compositional uniformity across 100 mm CdZnTe/GaAs using high resolution photoluminescence mapping	20
21	Tipping growth - morphology (400X), supersaturation 10K	22
22	Tipping growth - morphology (400X), supersaturation 5K	22
23	FTIR transmittance spectrum	23
24	Ga concentration as a function of depth	25
25	Ga concentration obtained from SIMS analysis is shown as a function of depth	26
26	Sources of substrate attack by melt	27
27	MG-WC-1 LPE substrates (alternate) ploy-GaAs contamination reduced and tracks directly with LPE carrier concentration	28
28	SIMS analysis shows a Ga concentration of about 3.0E15 atoms/cm^3, decreasing to 3.0E14 atoms/cm^3 near the substrate interface	29
29	The average dislocation etch pit density	30
30	80 K I/V curves for 60 μm x 60 μm mesas made on wafer AS017	31
31	A histogram of differential resistance at a bias of -20mV at 87K	31
32	The photoresponse as a function of wavelength for diodes at 80K, from which a cutoff wavelength of 8.6 μm is derived	32

LIST OF TABLES

		Page
1	Status for substrate parameters	1
2	Summary of CdTe film orientation on GaAs and GaAs/Si substrates with different misorientations	17
3	Results from the series of slider LPE base layer runs carried out on both Si-based and bulk CdTe substrates	24

1 PROGRAM GOALS AND STRATEGY

Our goal has been to develop a Si-based substrate production capability. This production facility should be capable of supplying LIRIS and others in the infrared community with an alternative to bulk CdZnTe substrates for HgCdTe detector fabrication. The substrates should be suitable for the growth of epitaxial HgCdTe epitaxial films with a residual impurity concentration and crystalline defect density that are comparable with those presently obtained using bulk CdTe substrates. Table 1 lists specifications that must be met for the substrates to reach this goal. Such substrates will offer reduced cost, increased size and availability, and greater ruggedness when compared with bulk CdZnTe substrates. They may also offer a reliability improvement resulting from the reduction of thermal expansion mismatch with the readout circuit.

Table 1 *Status for substrate parameters.*

Specification	Spire Substrates I Program	IRFPA II Goal	Status
Wafer Thickness	975 ± 10 μm	975 ± 10 μm	975 ± 10 μm
Wafer dimensions	20 mm x 30 mm	40 mm x 60 mm	20 mm x 30 mm
CdZnTe orientation	<111> B	<111> B	<111> B
CdZnTe composition	0.025 < x < 0.050	0.040 < x < 0.050	0.045 ± 0.002
CdZnTe film thick	15 μm < t < 20 μm	5 μm < t < 15 μm	7 μm ± 1%
X-ray rocking curve		200 arc sec	< 150 arc sec
Average transmit	> 55% 6-14 μm	> 55% 6-14 μm	> 55% 6-14 μm
Parallelism	< 1 μm/mm	< 1 μm/mm	< 0.5 μm/mm
Flatness	< 10 μm/90% wafer	< 10 μm/90% wafer	< 10 μm/90% wafer
Residual impurity (MCT)	< 5E15/cm^3	< 1E15/cm^3	< 2E15/cm^3
Defect density (MCT)	< 5E5/cm^2	< 5E4/cm^2	5E5/cm^2

Spire has functioned as a supplier of substrates and epitaxial materials to the semiconductor industry for many years. For this reason Spire's production and distribution skills, as well as their expertise in MOCVD equipment construction and process development, has made it possible to establish a supply of epitaxial CdZnTe/GaAs/Si substrates. The evaluation of Spire substrates for HgCdTe detector fabrication has been carried out at LIRIS by growing p-on-n HgCdTe heterostructures on these substrates and characterizing the structural and chemical quality of the epitaxial films by chemical and crystallographic means. A Te-rich slider LPE method was used for growth of the n-type films, and a Hg-rich dipper LPE method has been used

to grow wider gap p-type layers on the n-type base layers to form a grown p-n junction. Arrays of photodiodes have been fabricated from this material, and the optical response and diode characteristics measured and compared with those of devices fabricated on CdTe substrates using the same HgCdTe growth and processing methods.

The substrate production capability at Spire was funded, in the early phases, by the IRMP Phase I Program, Contract #MDA972-92-C-0039. The SPI-MOCVD™ 3000G reactor was brought into operation as part of the IRMP Phase I Program at Spire, and startup was assisted by a transfer of CdZnTe MOCVD growth technology from LIRIS. More recently, under the IRFPA II Program, LIRIS subcontract #2301001 has funded process development, while substrate and diode evaluation has been carried out at LIRIS. Design, construction, and installation of the SPI-MOCVD reactor was funded in part by the NIST-ATP Program, Contract #70NANB2H1257.

MOCVD growth was chosen for epitaxial growth of GaAs and CdZnTe because of the capability for simultaneous deposition on large numbers of wafers, resulting in low cost. While Spire has considerable experience in the growth of GaAs on Si, The MOCVD process for the growth of CdZnTe had to be developed, as did the growth of GaAs on the particular orientations required for high quality CdZnTe growth.

The SPI-MOCVD 3000G reactor is of a configuration that has been used for production of epitaxial Si, but had not previously been used for MOCVD of CdZnTe. Since the flow dynamics in MOCVD reactors have a major influence on deposit quality and both composition and thickness uniformity, we have used an MOCVD reactor modelling capability at MIT, under the direction on Prof. Klavs Jensen, to model MOCVD growth processes for both GaAs and CdZnTe in this reactor. Modelling efforts by this group have been useful in understanding GaAs growth in other reactor designs, and can greatly reduce development time for a new reactor design or process by predicting operating conditions that will lead to flow stability, as well as equipment modifications or flow conditions that optimize deposit uniformity. This work was carried out under subcontract #2300009 from the LIRIS IRFPA II Program.

The LPE process requires that the Si and GaAs layers be protected from the Te-rich melt by an encapsulant, since they are highly soluble in the melt and could contaminate both the melt and HgCdTe deposit. Development of this encapsulant as well as the MOCVD growth of both GaAs and CdZnTe layers on Si was carried out at Spire Corp. Evaluation of the effectiveness of the encapsulant and the quality of the substrate for LPE growth has been carried out at LIRIS by growth of single layers of HgCdTe, double layer p-n junctions, and by the chemical and electrical characterization of both single layers and grown junction photodiodes.

The present status is that a thermal oxide encapsulant has been developed that is impervious to the Te-rich LPE melt and is not wetted by it. This encapsulant has made it possible to reduce the Ga impurity level in LPE HgCdTe to below 1×10^{15} atoms/cm^3. At the same time it has been found possible to produce CdZnTe deposits with a (111) B orientation that are free of twins at the surface and are of excellent crystalline quality with dislocation densities of down to 5×10^5/cm^2 and an X-ray rocking curve FWHM of below 80 arc.sec. Long-wave infrared diodes with a quantum efficiency of 50% (when illuminated through the uncoated Si substrate) have been produced form this material.

2 RESULTS AND STATUS

2.1 Encapsulation

The encapsulants evaluated were as follows:

- silicon dioxide deposited by the reaction of SiH_4 with O_2 in a CVD reactor ("Silox")
- silicon nitride deposited from SiH_4 and NH_3 by plasma-enhanced CVD (SiN)
- silicon dioxide formed by heating the Si substrate to a high temperature (e.g. 1050°C) in a flowing O_2 atmosphere ("Thermal oxide")

The combinations SiN on silox and SiN on thermal oxide were also evaluated. The encapsulants were evaluated by measuring the pinhole density or by immersion in a molten Te-rich melt. Pinhole density measurements were carried out by immersing the wafers in molten KOH, which preferentially etched the Si where it could penetrate the encapsulant at pinholes, then etching away the encapsulant in HF solution to enable the etch pits marking the location of etchant penetration of the encapsulant to be counted. The number density of sites where penetration and attack had occurred was taken to be the density of pinholes in the encapsulant. The immersion experiments were carried out by placing encapsulated wafers in molten Te-rich LPE melt for 1 hour at 500°C, then removing them from the melt, cooling to room temperature, and examining them for indications of attack by the melt.

Pinhole densities were found to be a function of the encapsulant deposition process conditions, and of the encapsulant thickness. Figures 1 and 2 show data indicating that for silox films the pinhole density decreased as the deposition temperature increased up to 450°C, the practical upper limit for the deposition system used, and that a thickness of at least 1.5 μm was the optimum. The average pinhole density obtained for silox in this series of experiments was, under optimum conditions, about $1000/cm^2$. Figures 3 and 4 show data that indicate, for SiN films, the optimum deposition temperature was at 400°C or higher and the optimum film thickness was at 0.1 μm or below, with resulting pinhole densities of less than $500/cm^2$. Figures 5 and 6 show data for thermal oxide that indicates that oxidation at 950°C to a film thickness of 0.2 μm results in an average pinhole density of $<100/cm^2$. Figure 7 shows data for three wafers with a combination thermal oxide plus nitride and three wafers with a combination of nitride and silox. These results show, surprisingly, that the combination encapsulants have a pinhole density very similar to that of the first deposited film, so that they offer no advantage over single films.

Melt immersion experiments were carried out on 2 cm x 3 cm wafers totally encapsulated with thermal oxide, SiN, SiN plus silox, and thermal oxide plus SiN. These wafers were immersed in the LPE melt at 500°C for 60 m, then the melt was poured off by tilting the ampul. The results confirmed the conclusions drawn from pinhole density measurements in that the thermal oxide encapsulated wafer showed least attack, with only minor dissolution of areas around the edge. All of the other wafers showed dissolution of from 5 to 20% of the wafer area. Encapsulant failure resulted primarily because the SiN showed extensive peeling from both the SiN encapsulated and thermal oxide plus SiN encapsulated wafers. In the case of the thermal oxide plus SiN encapsulated wafer the SiN peeling process damaged the underlying thermal oxide, resulting in melt penetration.

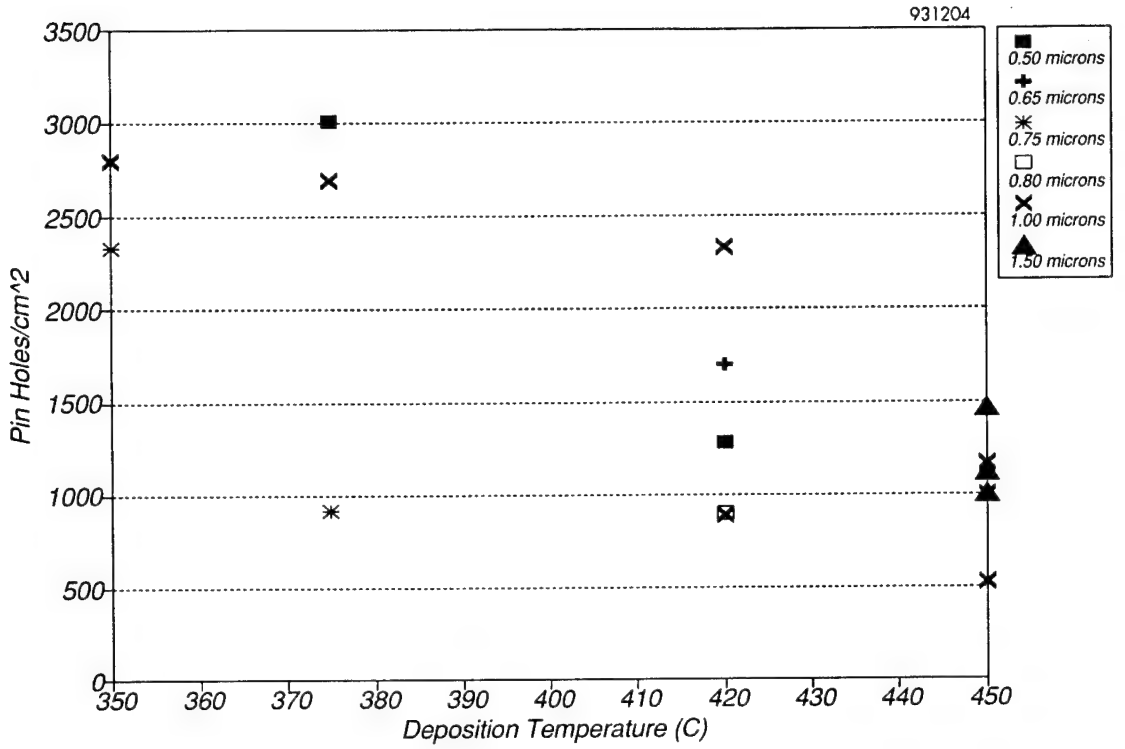


Figure 1 *Single layer SILOX encapsulation, silicon wafers (deposition temperature).*

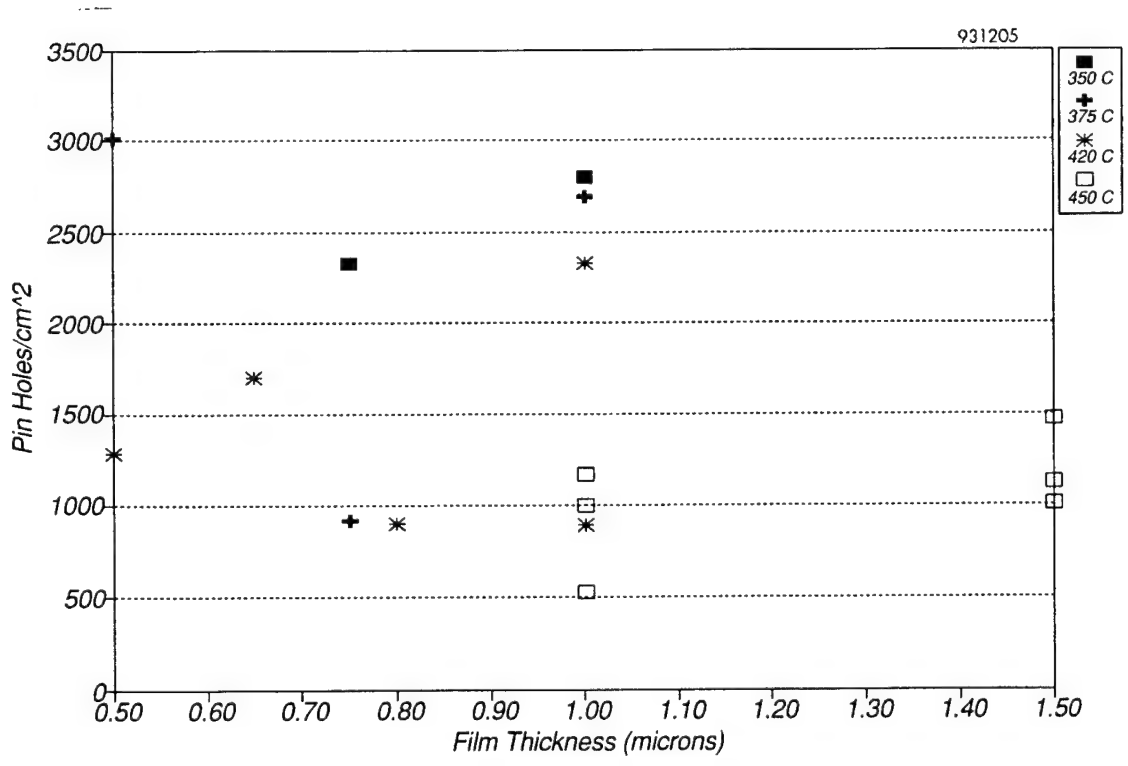


Figure 2 *Single layer SILOX encapsulation, silicon wafers (film thickness).*

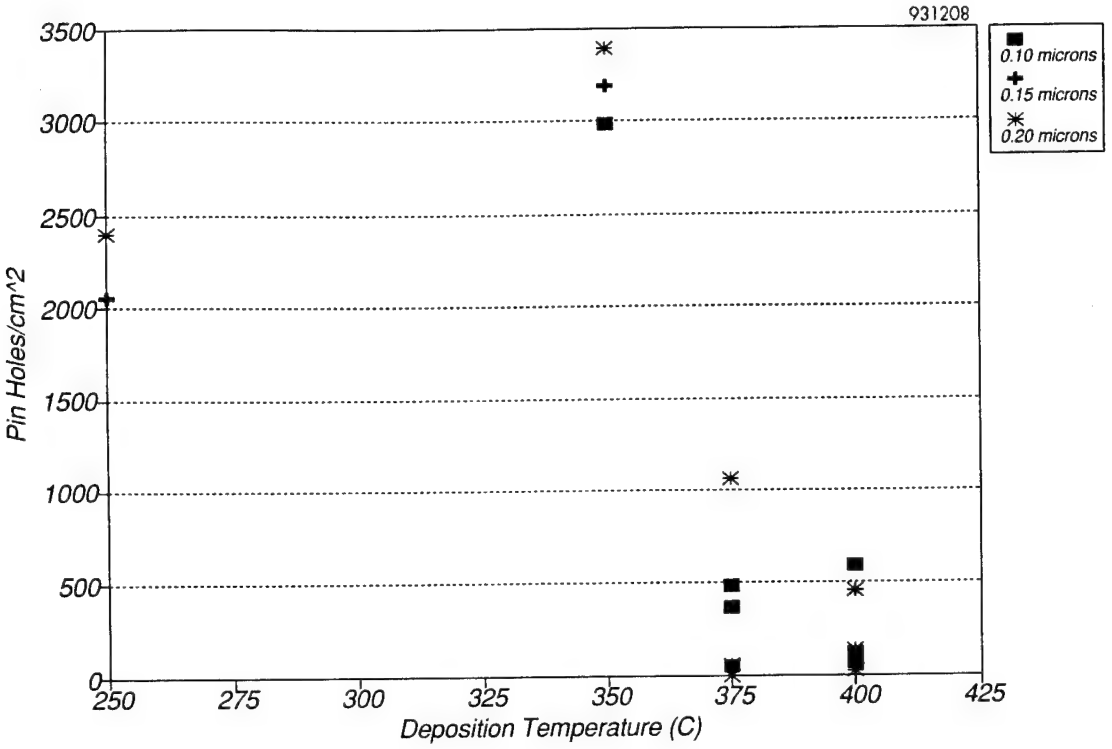


Figure 3 *Single layer nitride encapsulation, silicon wafers (deposition temperature).*

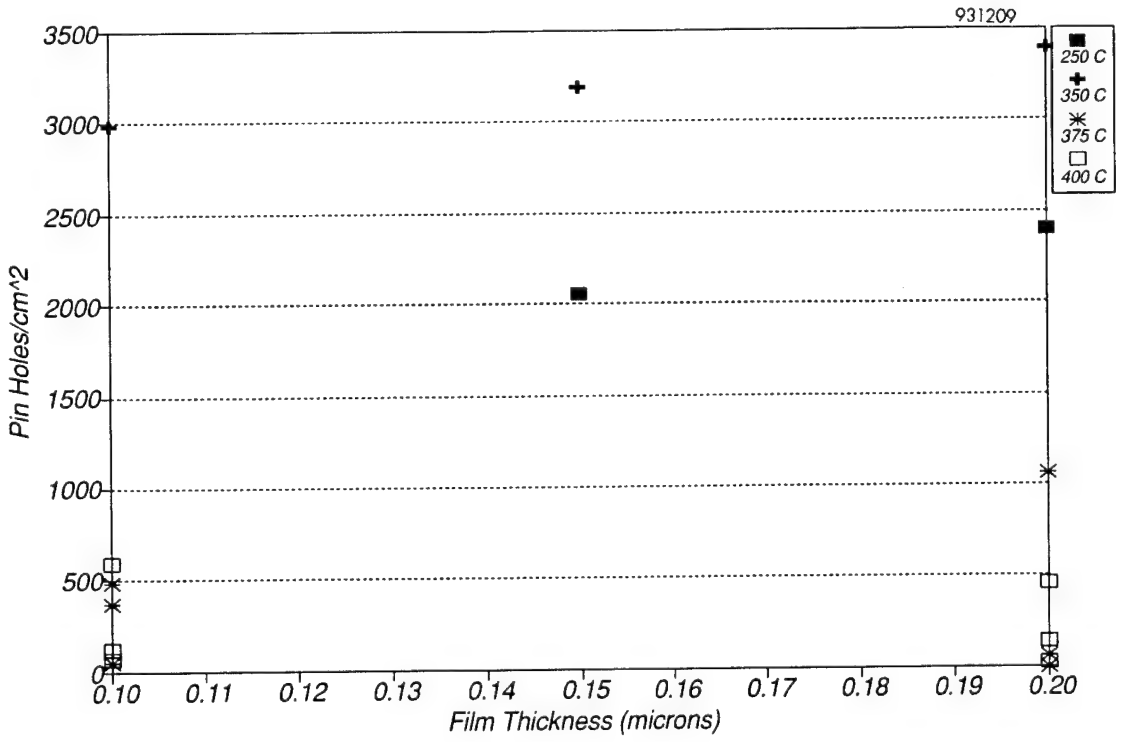


Figure 4 *Single layer nitride encapsulation, silicon wafers (film thickness).*

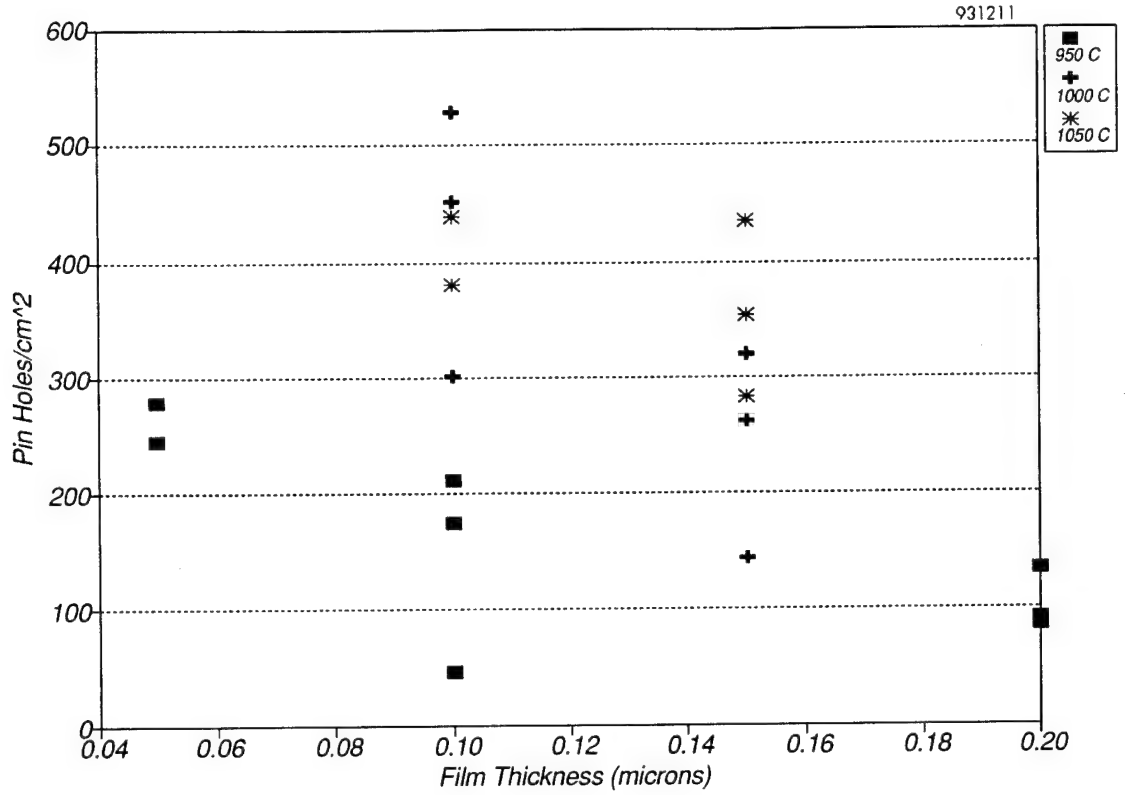


Figure 5 *Single layer thermal oxide encapsulation (deposition temperature).*

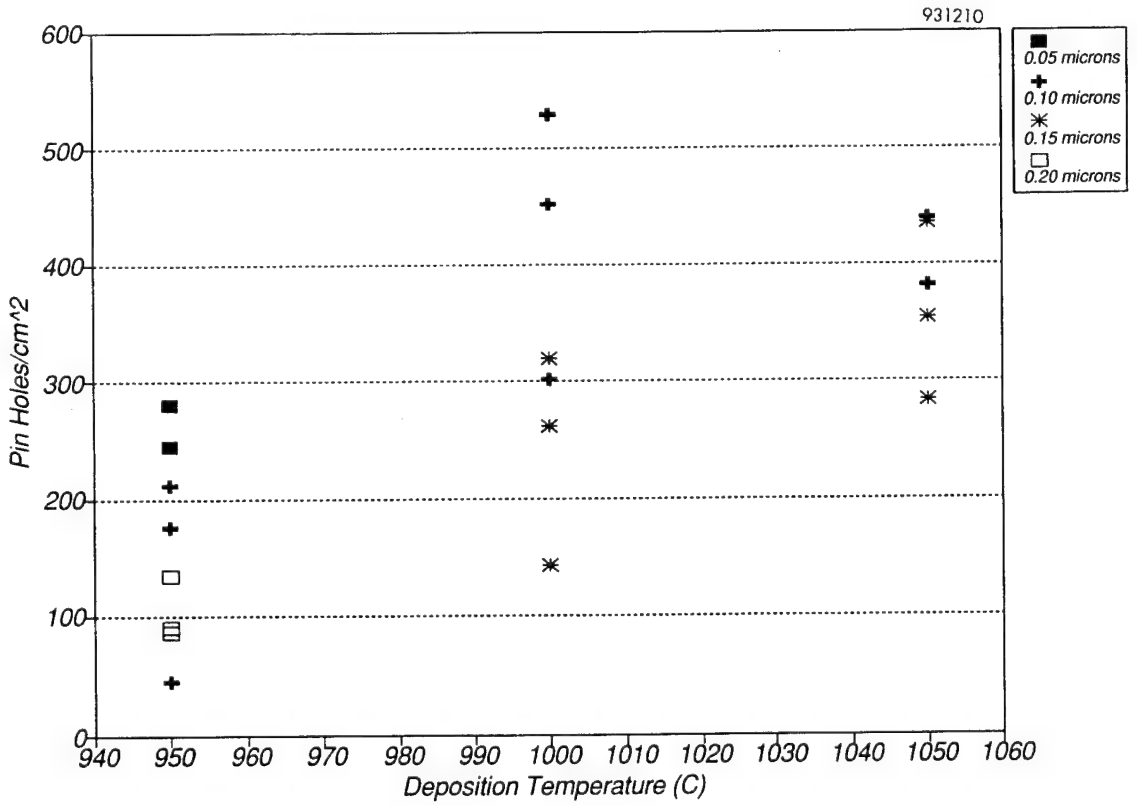


Figure 6 *Single layer thermal oxide encapsulation (film thickness).*

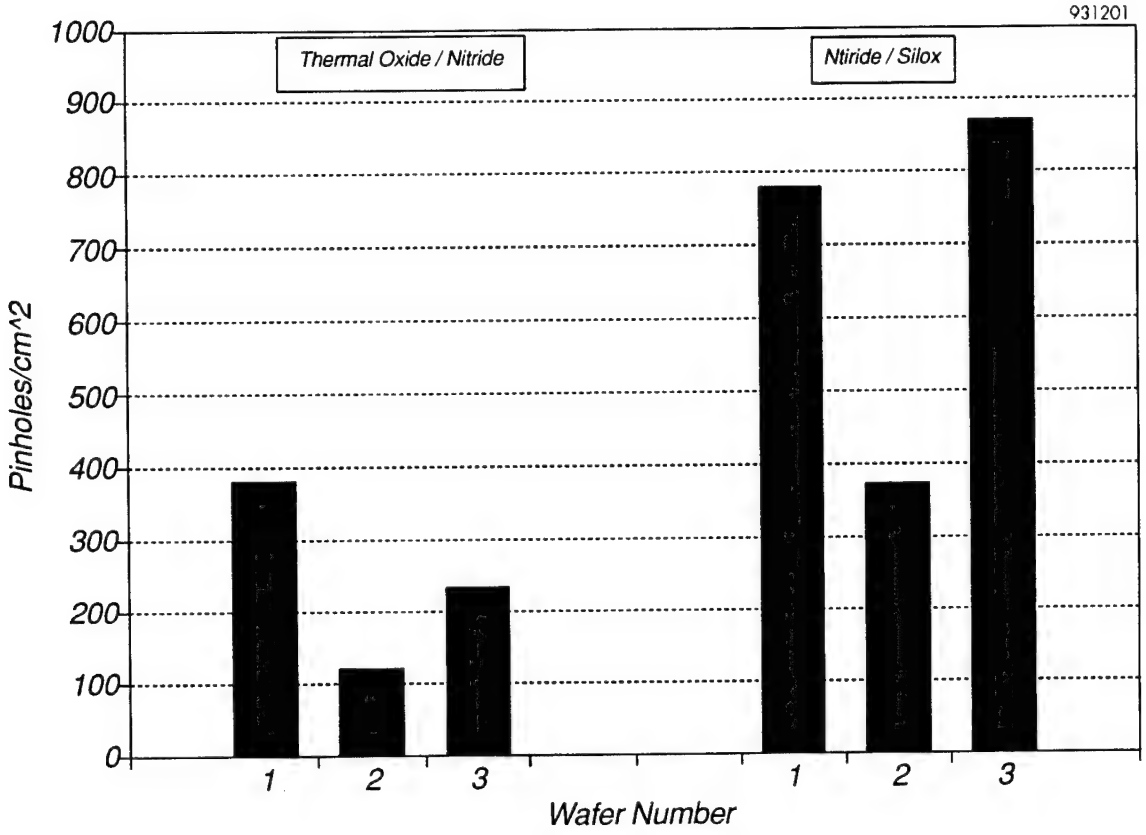


Figure 7 *Two layer encapsulation summary, silicon wafers.*

It was hypothesized that edge attack, seen even in the case of the wafer encapsulated with thermal oxide only, resulted from incomplete coverage at sharp corners and edges formed when these wafers were cut from 3 inch diameter silicon wafers with a diamond saw. Efforts were therefore made to improve the smoothness of the diamond sawcuts and to round the edges of wafers after sawing and prior to encapsulation. A brief investigation of laser cutting did not show any promise as a method of obtaining a smoother edge profile than is obtained by diamond saw cutting. The edge rounding methods applied to saw-cut wafers were as follows:

- mechanical edge-rounding on a rotating disk using a diamond paste abrasive
- micro-bead blasting the edges, either with or without a chemical polish after rounding
- chemical edge-rounding by immersing the cut edges in one of the known chemical polishes for Si, i.e. a 12:1:1 mixture of nitric, hydrofluoric, and acetic acid.

Mechanical edge rounding was found to work satisfactorily, but was tedious and time consuming, not an acceptable production method. Micro bead-blasting gave good edge rounding but resulted in considerable damage to the polished wafer surface. It would therefore have to be carried out prior to final polishing of the wafer surfaces. Chemical edge-rounding also damaged the wafer surfaces, but appeared to be the best option for production scale use.

A second series of 6 melt-immersion experiments were carried out using thermal oxide encapsulated wafers that had been mechanically edge-rounded. Thermal oxides were grown at

either 950°C or 1200°C to a thickness of 2250Å. No attack of these wafers, either at the edges or on the polished surfaces, was seen after immersion in Te-rich LPE melt at 500° for 60 minutes.

Subsequent LPE growth experiments have shown that chemical edge-rounding after sawing and before double-sided polishing, followed by thermal oxidation at 1050°C, results in an encapsulated wafer that is impervious to the Te-rich LPE melt at temperatures up to 500°C. It is probable that the use of standard round Si wafers, which are supplied with the edges rounded, would not require any rounding of the wafer edges prior to oxidation.

One of our concerns about Si substrates was to maximize transmittance in the region of interest. The two major causes of optical absorption in the infrared for Si wafers are free-carrier absorption and a band due to Si-O vibrations at about 9 μm in Si containing O. High resistivity p-type Si was used to minimize free carrier absorption, and zone refined Si was used since this has a much lower O content, and therefore less absorption at 9 μm, than the more usual Czrochralski-grown material. This resulted in a transmittance of about 60% throughout the 3 μm to 11 μm region, primarily limited by reflectance at the uncoated surfaces. The encapsulants themselves absorb strongly at about 9 μm but, since they are removed completely from the finished detector by etching, this is not of concern.

2.2 Wafer Bow

Encapsulant materials are widely known, from silicon technology literature, to be under stress in the as-deposited condition. The magnitude of this stress is a function of the deposition process, particularly for SiN films. Additional stress results from the difference in thermal expansion coefficient between the Si substrate and the deposited film during cooling from deposition temperature. Since these stresses result in bending of the Si substrate when the encapsulant is on only one side of the wafer, difficulty could be encountered in slider LPE growth as a result of the need to maintain close spacing between the substrate and the graphite boat. Deposited GaAs and CdZnTe films also cause the wafer to bow. At LPE growth temperature, the difference in thermal expansion coefficients between the various layers of the structure will change the amount of bow, making it difficult to achieve a flat wafer at both room temperature and at growth temperature. Once bowing effects of the various components are known, it should be possible to use deposited dielectric films, for both encapsulation and bow control.

In order to assess the bowing affect of deposited films, the amount of bow was measured for 25 Si wafers, 4-inch diameter, both before and after deposition of thermal oxide, Silox, SiN, and thermal oxide plus Silox. Bow was measured using a Rodenstock Laser Profilimeter to determine the height of the surface of an unrestrained wafer sitting on a horizontal steel block. Various thicknesses of deposited films were investigated. Figure 8 shows the amount of bow found for various thicknesses of thermal oxide and SiN. The thermal oxide films were all in compression. The SiN films were in tension, and for both oxide and SiN the amount of bow increases with film thickness, as expected. Silox films were all in compression but did not cause as much bow as did the thermal oxide. These results indicate that wafer bow of either sign can be balanced by a film of either thermal oxide or SiN on one side of the wafer. The amount of bow observed was, in all cases, less that the 10 μm maximum established as a specification for either Si-based or conventional substrates. After growth of HgCdTe films 15 μm to 25 μm thick less than 5 μm bow of 2 cm x 3 cm Si-based substrates was observed.

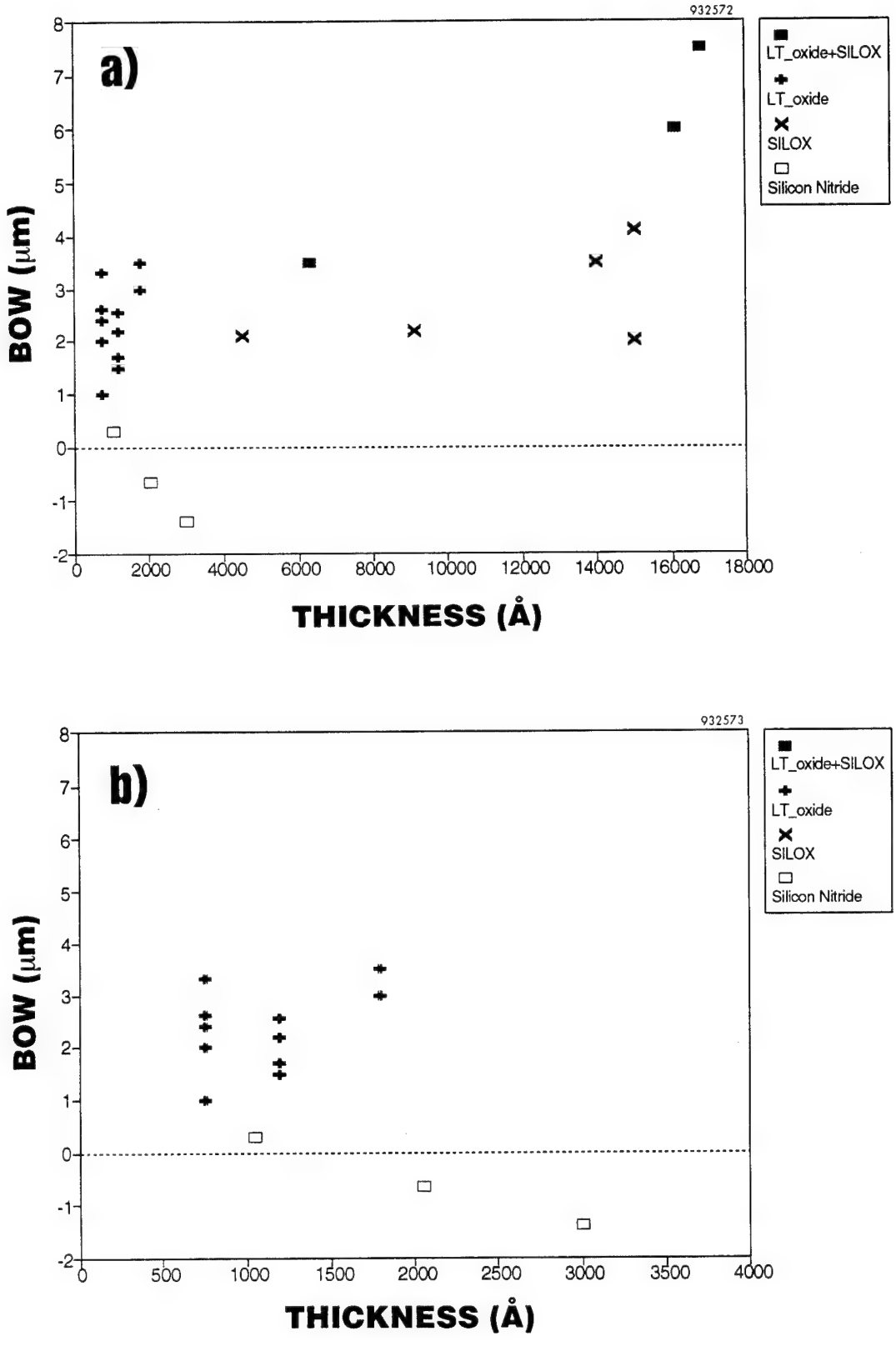


Figure 8 *Variation of bow in Si for different encapsulants a) thick layers and b) thin layers.*

2.3 The MOCVD Reactor

All CdZnTe films were deposited in Spire's 3000G large barrel-type reactor, shown schematically in Figure 9. This reactor formed one side of a pair of similar reactors placed next to each other in a class 100 clean room, as shown in Figure 10. Details of the MOCVD reactor and deposition are shown in Appendix A. These two reactors shared a common power supply and so could not be operated simultaneously. The second reactor was equipped for the growth of GaAs films. Most of the GaAs films used for the present program were grown in a Spire model 450 reactor since the GaAs/Si process is well known for this reactor at Spire, and because the 3000G reactor power supply was constantly in demand for the growth of CdZnTe. GaAs films were grown from trimethylgallium (TMGa) and arsine, CdZnTe films were grown from dimethylcadmium (DMCd), dimethyltellurium (DMTe) and diethylzinc (DEZn). In a typical CdZnTe deposition sequence the GaAs/Si substrate is first exposed to a short pre-growth bake to remove the native oxide, this is followed by deposition of CdZnTe at about 420°C with a reactor pressure of about 400 torr, at a deposition rate of about 6A/s.

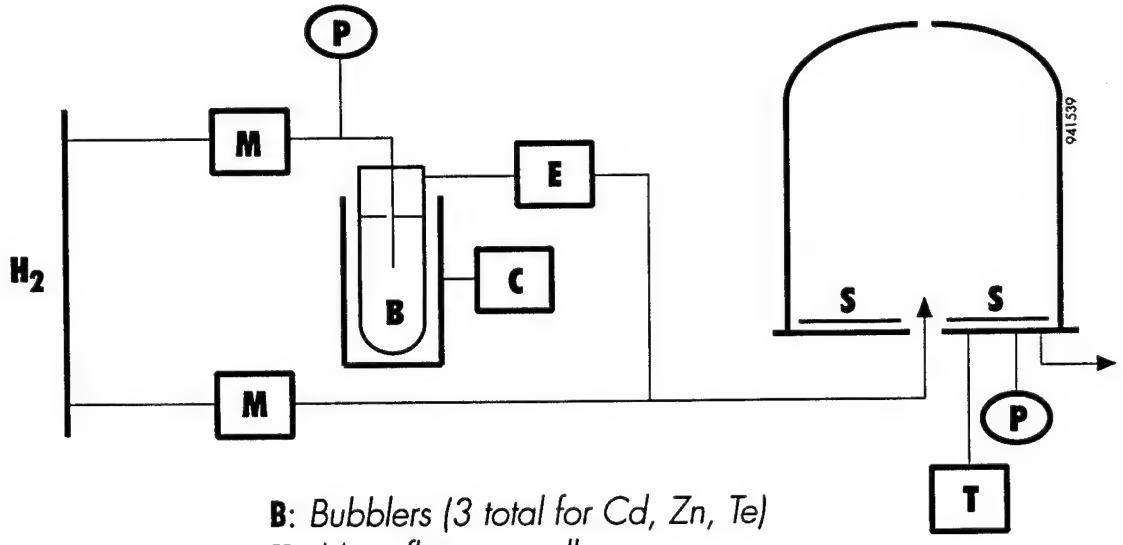


Figure 9 *Spire SPI-MOCVD™ 3000G MOCVD reactor (all sensors input through A/D to control CPU).*

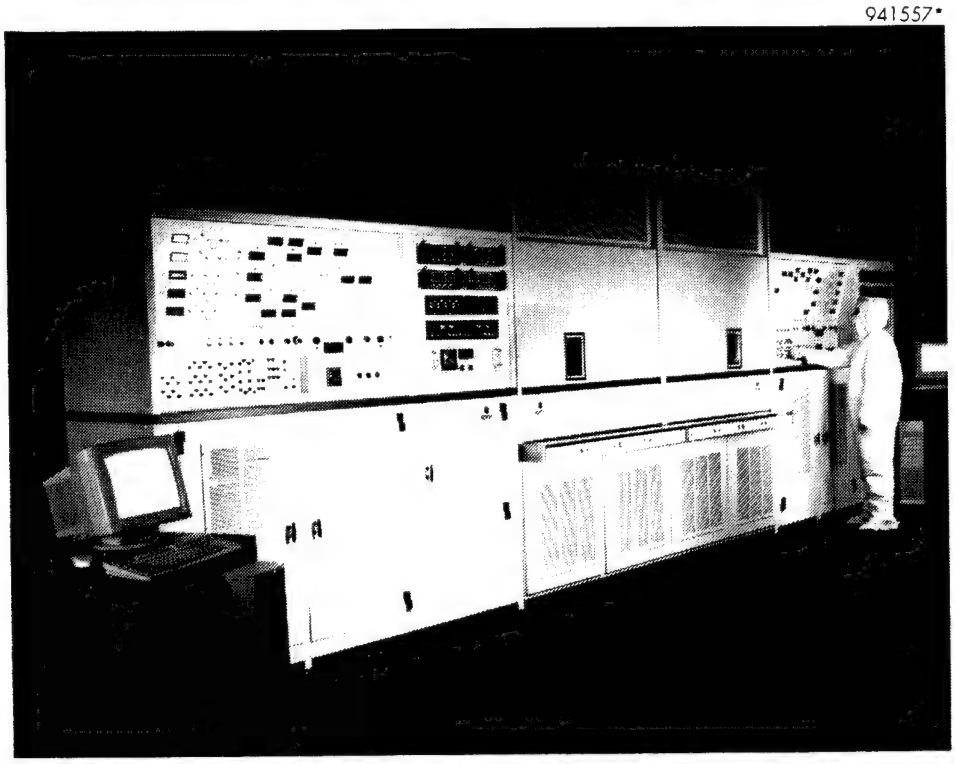


Figure 10 *SPI-MOCVD 3000 G reactor.*

The 3000G reactor was equipped with Epison gas concentration monitors on the DEZn, DMCd and DMTe supply lines, making it possible to continuously monitor the concentration of these vapors in the hydrogen carrier gas. In this way change in the vapor concentration of these components, due to depletion of the bubblers used to supply them for example, could be corrected. Mass flow controllers were used to supply the hydrogen carrier gases at a well-controlled rate so as to ensure reproducible conditions in the reactor. The temperature of the wafer platen is monitored by an optical pyrometer. Figure 9 shows schematically the sensor and control system for the 3000G reactor.

The Spire 450 reactor has a capacity of three 3-inch diameter wafers, with a typical run time of about 4h. The capacity of the 3000G reactor is about fifteen 3-inch or ten 4-inch wafers per run, a typical run takes about 5h. The large capacity of the 3000G reactor would not be useful unless a high degree of wafer-to wafer uniformity can be achieved, so that a high yield is obtained. Obtaining a uniform deposition rate in a CVD reactor is difficult because gas flow patterns are set up that, together with reactant depletion, result in variations in reactant feed rate across a group of wafers. In order to reach an understanding of these effects, and in order to make it possible to calculate conditions under which depostion rate uniformity would be optimized, a model for the deposition process in this reactor was developed by K. Jensen and P. Futerko, of the MIT Chemical Engineering Department.

2.4 The Reactor Model

MOCVD growth is a complex process and one that requires a large number of runs to optimize. This is particularly true in the case of a reactor geometry that has not previously been

used for II-VI compound growth, and for growth of compounds such as CdZnTe for which there is much less literature than for the III-V compounds such as GaAs. The reactor temperature, pressure, total flow rate, concentrations of the 3 reactants, and film nucleation conditions must all be treated as variables, so that several hundred experiments are required to reach optimum operating conditions. The number of experiments can be reduced if a reliable computer model of the reactor can be constructed, provided it can be verified by a relatively small number of experiments, and used to predict optimum operating conditions. A reactor modelling effort was therefore carried out at MIT by K.F. Jensen and P. Futerko.

The first step taken in the program to model the 3000G reactor was to model fluid flow and heat transfer using the Galerkin finite element method, assuming the flow to be laminar. In order to test this model the temperature of the reactor wall was calculated for a few wafer-holder temperatures. The wall temperature was also measured at Spire, with these wafer holder temperatures, for comparison of the calculated and experimental values. Figure 11 shows a comparison of the calculated and measured wall temperatures.

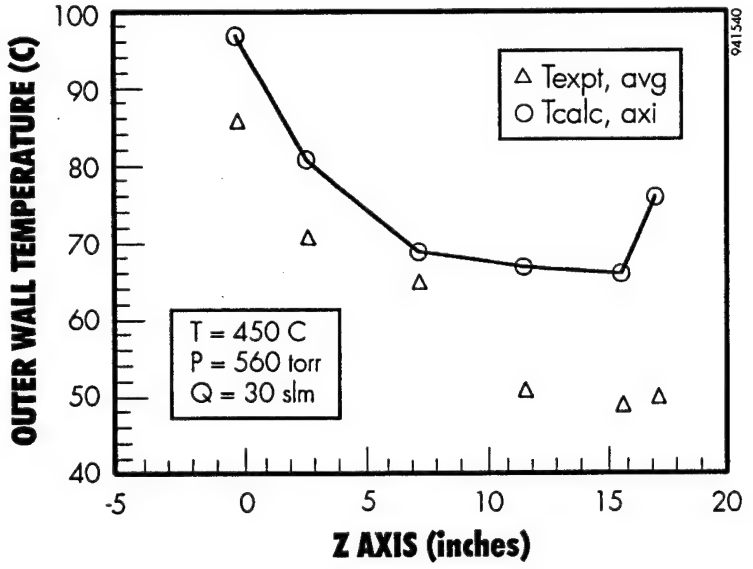


Figure 11 *Comparison of calculated and average experimental temperatures of the outer wall.*

As can be seen, although the agreement is reasonable for distances of up to eight inches above the level of the wafers, near the top of the reactor the predicted temperature rises in a way that is not duplicated in the experimental data. Figure 12 shows gas flow streamlines predicted for the reactor under conditions similar to those used in a CdTe deposition run. When the deposition rate of GaAs was calculated from this model, using the well-known rate constants for the reactants used, a very steep dependence on radial position across the wafer carrier was predicted, as shown in Figure 13. The position dependence of the deposition rate was similar whether the TMGa was considered to be decomposed to Ga and incorporated into the crystal lattice at the substrate surface ("model 1" in Figure 13) or to be decomposed in a step-wise fashion in the gas phase with adsorption of decomposition products onto the substrate surface ("model 2").

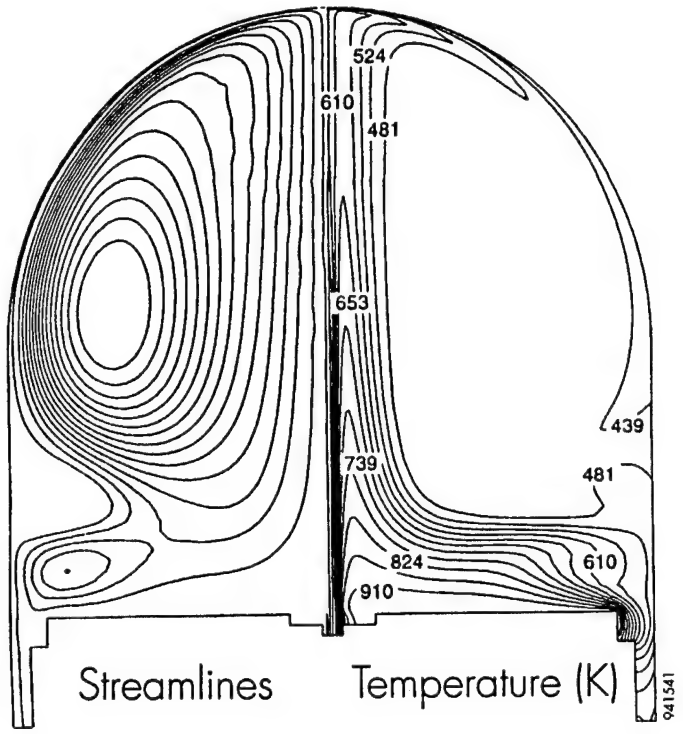


Figure 12 *Gas flow streamlines predicted for the reactor under conditions similar to those used in a CdTe deposition run.*

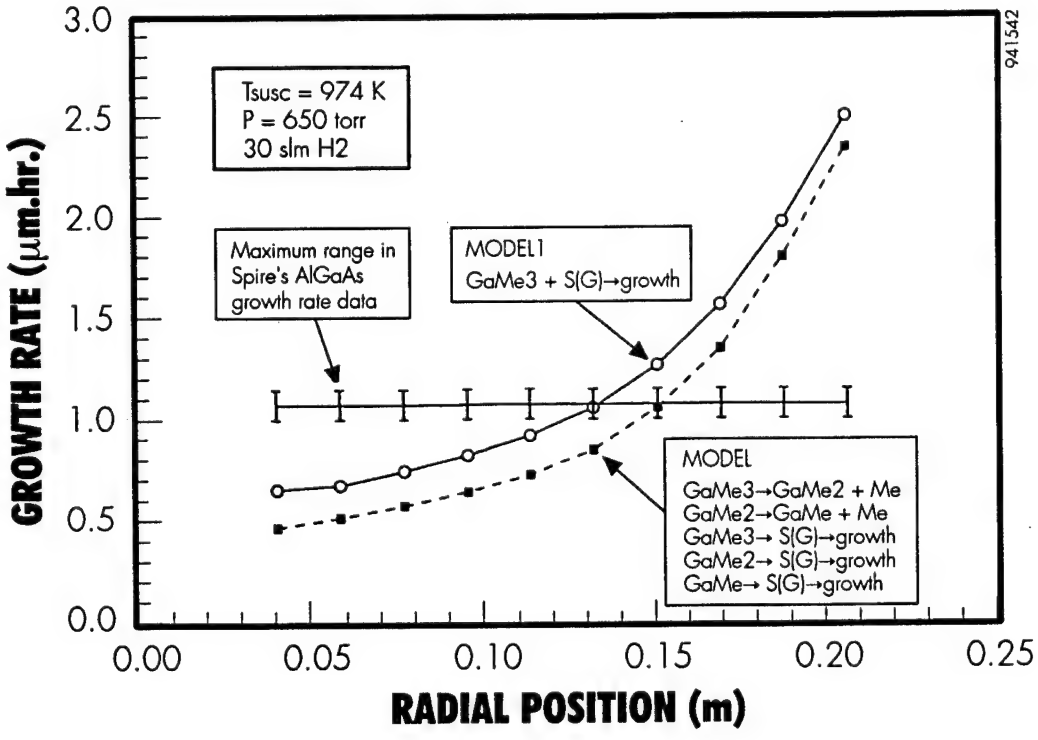


Figure 13 *Comparison of calculated growth rates with experiments.*

As a result of this poor agreement of the model with the experimentally determined reactor wall temperature and growth rate uniformity the possibility that , because of the large size of the reactor, the flow is at least partially turbulent, *i.e.* chaotic was considered. Turbulence would increase reactant mixing in the region above the susceptor, resulting in a more uniform growth rate, as observed. A method for modelling turbulent flow in a finite element framework was therefore implemented. This is a much more difficult problem than for the laminar flow case, and even in a simple cylindrical geometry the model was found to be extremely time-consuming to solve. A simplified turbulence model was therefore used to capture the important aspects and results of turbulence in the Spire reactor.

In the simplified model of the reactor, it was assumed that the core is fully turbulent while within a boundary layer near the walls it is laminar. Transport properties within the turbulent core were then obtained from a turbulent eddy viscosity. Predictions of the reactor wall temperature and deposition uniformity were then compared with experimental data. Figure 14 shows a comparison of the experimental and predicted reactor wall temperatures. As can be seen, excellent agreement is obtained for the turbulent flow model. Figure 15 shows a comparison of the predicted deposition rates as a function of radial position in the reactor for the laminar and turbulent flow models under typical operating conditions. The turbulent flow model again gives results in good agreement with the experimentally observed uniform deposition rate, as shown in Figure 13. The absolute value of the growth rate is only about 0.2 Mm/h if unity sticking coefficient of the TmGa on the reactor wall is assumed, much lower than the observed rate of 1.1 μm/h. If an activation barrier of 15 kcal/mole is postulated to inhibit GaAs deposition at the reactor walls a growth rate that equals the experimental value is obtained. Figure 16 shows the predicted streamlines for the turbulent model of the reactor.

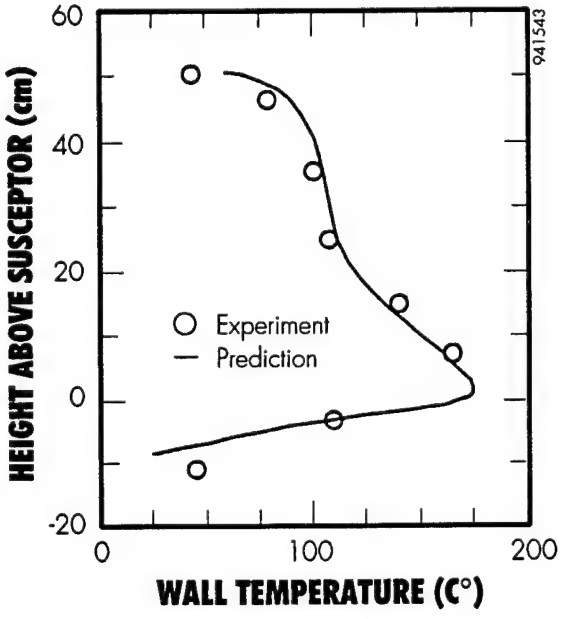


Figure 14 *Comparison of the experimental and predicted reactor wall temperatures.*

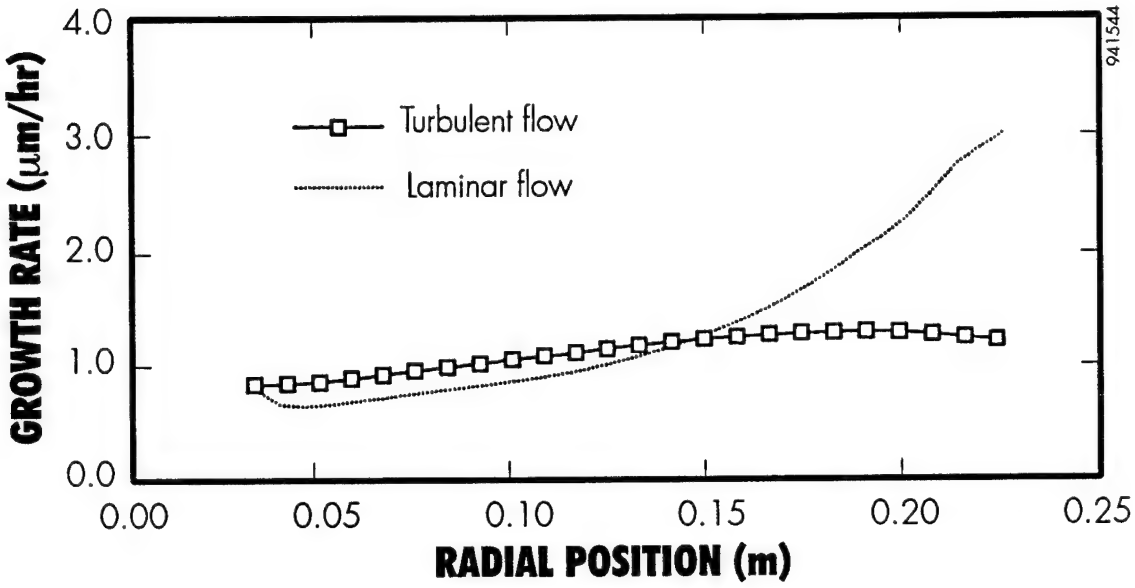


Figure 15 *A comparison of the predicted deposition rates.*

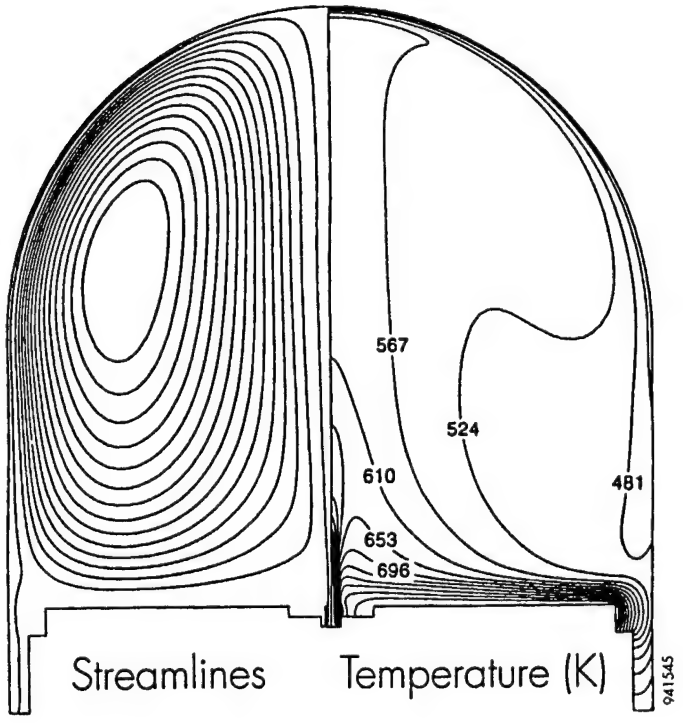


Figure 16 *Predicted streamlines for the turbulent model of the reactor.*

2.5 MOCVD Growth

It is possible to grow either (111) or (100)-oriented CdZnTe films on (100)-oriented GaAs/Si substrates. The introduction of DEZn prior to the start of growth, or the growth of a thin layer of ZnTe before beginning growth of CdZnTe, results in the (100) orientation, whereas initial growth of CdTe results in the (111)B orientation being obtained. The (111)B orientation has been found to give the best quality LPE HgCdTe films on bulk CdZnTe substrates, and is also a closer lattice match to the (100) GaAs surface than is (100) CdZnTe. The overall mis-match between Si and CdTe is reduced from 19% for the (100) orientation to 3.4% along one of the (211) directions in the CdTe lattice for the (111) orientation. This may be expected to lead to a reduction in defect density in the CdZnTe for this orientation. The major difficulty with use of the (111) orientation in the past has been the formation of twins, in particular columnar twins that propagate up to the surface of the film. Lamellar twins also form parallel to the film surface, but they are less of a problem since they do not intersect the surface and so would not nucleate a twin in a HgCdTe layer grown on the substrate. One of the major challenges in the present program was to obtain CdZnTe/GaAs/Si substrates free of columnar twins, since this is the optimum orientation for the LPE process.

Several Si wafer orientations close to (100) were investigated, as were various deposition conditions, to obtain CdZnTe films with a good surface morphology, low defect density, and free of columnar twins. The Si wafer orientations investigated were 0, 2, 4, 7, and 10° off (100) toward the [111] or [110] directions. It was found that the VI/II gas concentration ratio had to be optimized for each orientation to optimize surface morphology. A baseline 1 μm thick GaAs buffer layer was used for all substrates.

Figure 17 shows typical surface morphology as a function of silicon substrate misorientation and growth temperature for CdZnTe films (5 to 10 μm thick) grown on GaAs substrates. In all cases the misorientation of the Si substrate was toward the [111] direction. As expected, the morphology and surface roughness varies with substrate orientation. Films deposited on substrates with a misorientation of less than 2° had relatively smooth surfaces while those with misorientations in the range 4° to 10° had regular surface features that were independent of film thickness. The surface morphology was also a function of the growth temperature. At 460°C, CdZnTe films grown on 4° misoriented substrates showed a faceted surface with aligned triangular hillocks, films grown at 420°C were much more planar.

A study of the orientation of the GaAs and CdZnTe films grown on misoriented Si substrates was carried out by M.T. Leonard at The University of North Carolina, under the direction of Prof. N.A. El-Masry, using the Laue back-reflection geometry. Table 2 summarizes the results. In general the CdZnTe films are tilted further from the exact (111) orientation than the Si was misoriented from (100), by an amount that increases to about 2° for a 10° misorientation, so that for a Si misorientation of 10° from (100) the CdZnTe is mis-oriented 12° from (111).

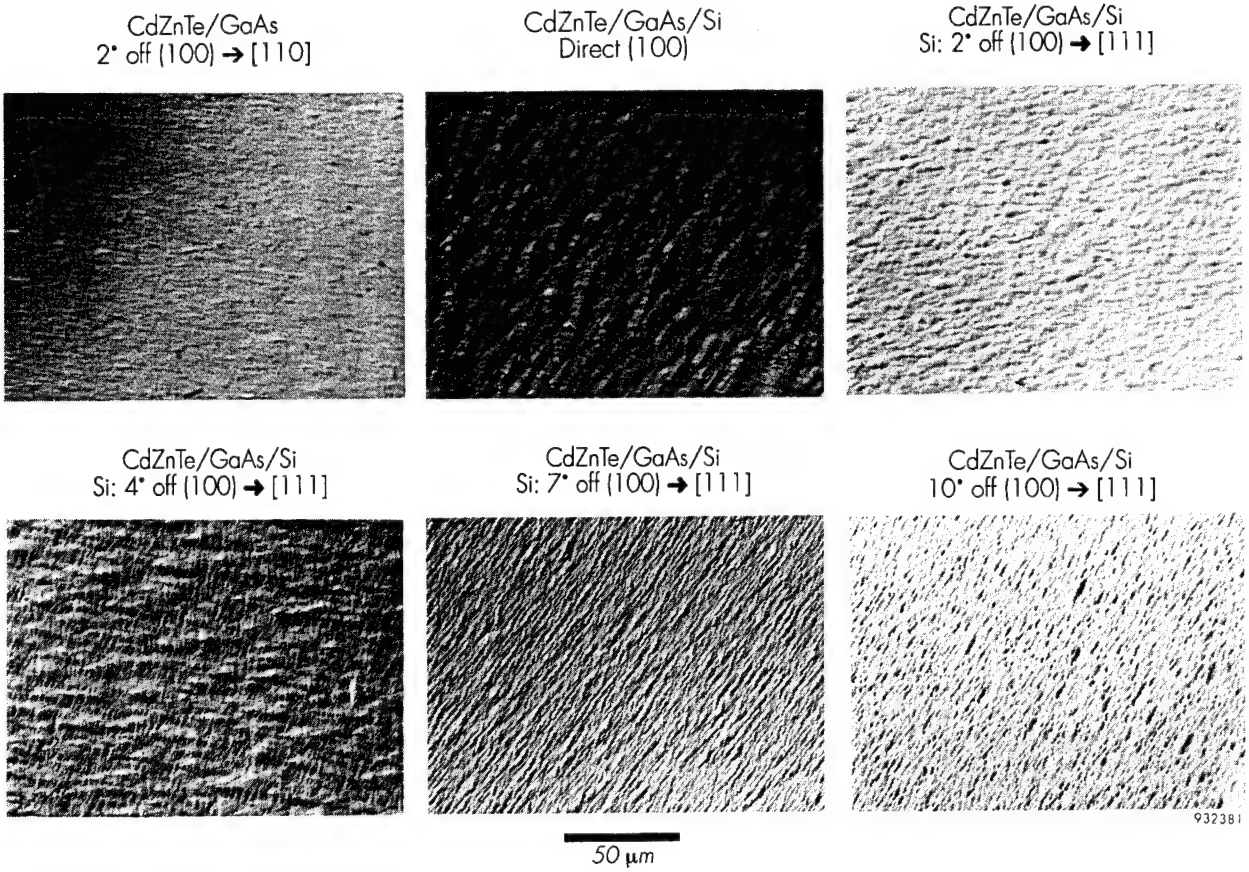


Figure 17 *Surface morphology for CdZnTe films deposited on GaAs and GaAs/Si substrates with different orientations.*

Table 2 *Summary of CdTe film orientation on GaAs and GaAs/Si substrates with different misorientations.*

Sample #	Substrate Orientation	Substrate Orientation (Laué)	Film Orientation
G26-0035-4	Si (100) off 2°	(100) off 4° → [111]	(111) off 5° → [111]
G26-0027-2	Si (100) off 4°	(100) off 4° → [111]	(111) off 5° → [111]
G26-0035-2	Si (100) off 7°	(100) off 7° → [111]	(111) off 9° → [111]
G26-0091-5	Si (100) off 10°	(100) off 10° → [111]	(111) off 12° → [111]
G26-0006-1	GaAs (100)	exact (100)	exact (111)
G26-0013-1	GaAs (100) off 2°	(100) off 2° → [110]	(111) off 2° → [110]
G26-0064-2	GaAs (100) off 2°	(111) off 2° → [110]	(111) off 2° → [110]
G26-0065-2	GaAs (100) off 2°	(111) off 2° → [110]	(111) off 2° → [110]

Cross-sectional TEM and X-ray diffraction were used to detect twinning in the CdZnTe layers. Figure 18 shows TEM micrographs for CdTe/GaAs/Si structures as a function of the substrate orientation. For a Si misorientation 2° off the (100) towards the [111], thin lamellar twins are formed parallel to the CdTe/GaAs interface. Twins form in the early phases of growth but stop forming once a few microns of CdTe have been grown. Small Angle Diffraction (SAD) was used to study the twinning phenomenon. SAD patterns near the CdTe/GaAs interface show extra diffraction spots due to the presence of twins, while near the surface these extra spots are absent. Lamellar twins are confined to a narrower region close to the CdTe/GaAs interface for 7° mis-oriented substrates. No rotational twins propagating perpendicularly to the film surface were seen.

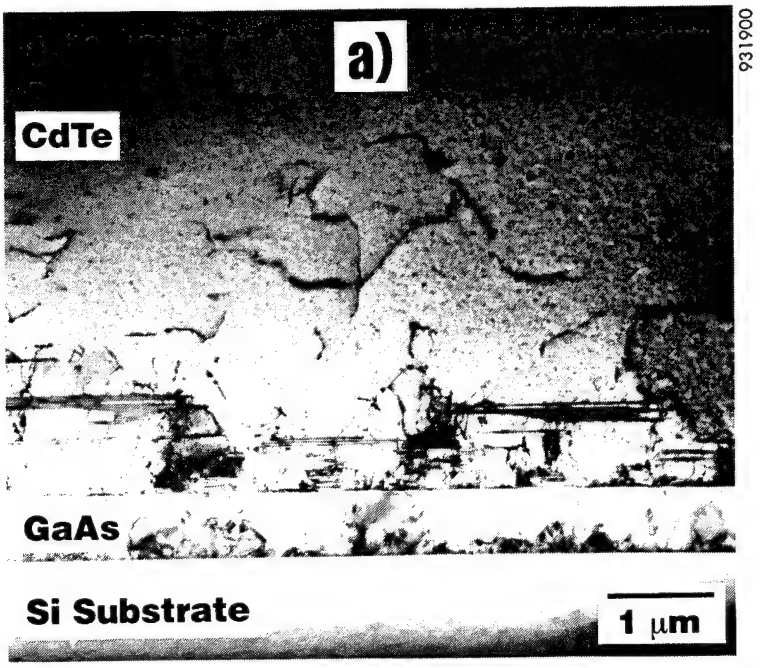
Thickness and composition uniformity of CdZnTe was excellent using the #3000G reactor. To determine the thickness uniformity of CdZnTe, films were grown on several three and four inch wafers in a single run. GaAs wafers were placed on the susceptor in such a way that uniformity across the entire susceptor could be obtained. Optical reflectance was used to measure the film thickness. Thickness was measured at 13 points on the three inch and 21 points on the four inch wafers. Figure 19 shows the thickness uniformity of a CdZnTe film on a four inch GaAs substrate. A standard deviation in thickness of 1% or less was obtained for the 6 wafers for which measurements were made. A standard deviation of less than 1% in wafer-to-wafer thickness was also obtained for these 6 wafers, all coated in the same run.

To determine compositional uniformity, room-temperature photoluminescence mapping measurements were done on CdZnTe films grown on GaAs substrates. These measurements were carried out at SCANTEX. Line scan peak wavelength measurements were performed at 200 points across the four-inch wafer. Figure 20 shows the variation of peak wavelength across a four-inch wafer. The composition variation was determined from the peak wavelength, and a range in Zn Composition of about 0.002 atom fraction was estimated for an average composition of about 0.04 atomic fraction of Zn.

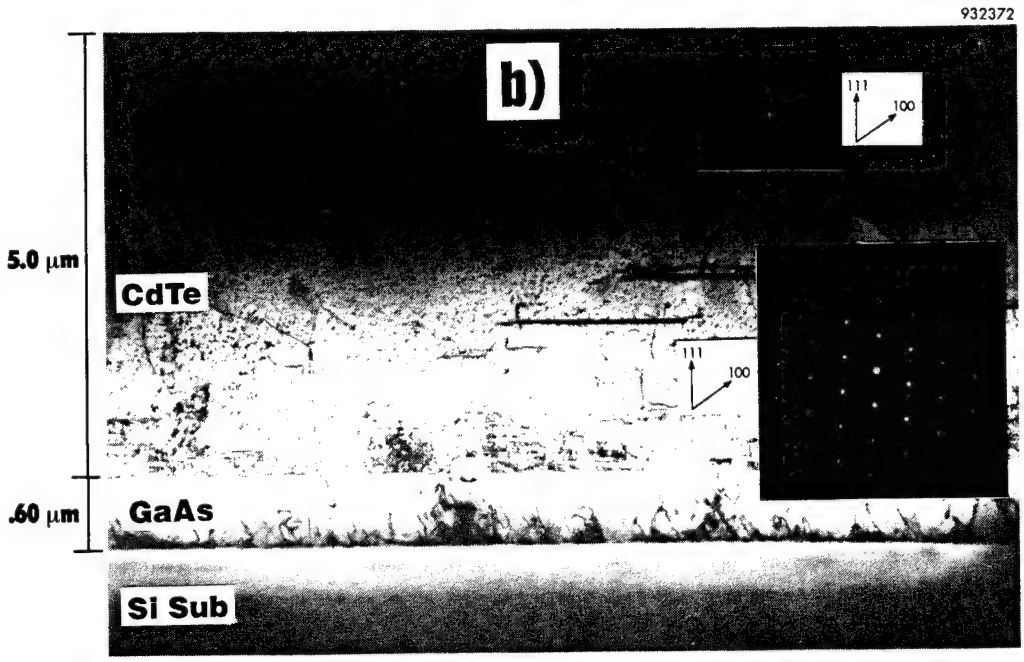
The Zn incorporation rate was found to be a function of both the substrate orientation and VI/II ratio in the inlet gases. For a VI/II ratio of 1.5 the Zn concentration increased it increasing DEZn/DMCd ratio. The Zn concentration was found to lower for CdZnTe films deposited on GaAs/Si as compared with bulk GaAs substrates. It was therefore necessary to re-determine the correct value of this ratio for each type of substrate.

2.6 LPE Growth of HgCdTe

Because of concern that encapsulant failure would lead to major contamination of both the LPE melt and equipment, initial growth experiments were carried out in a sealed quartz ampul. Three 2 cm x 3 cm CdZnTe/GaAs/Si substrates were held at one end of an evacuated and sealed 36 mm ID quartz ampul and sufficient Te-rich melt was held at the other end to totally immerse the wafers when the ampul was inverted. Several small CdTe source wafers were held at the melt end of the ampul and retained there by a coarse quartz screen when the ampul was tipped. The substrates were held in 4 mm wide slots in a solid quartz cylinder that was a close fit in the ampul and that was held in place by dimples in the ampul formed after the sealing operation. This quartz cylinder served to reduce the free volume around the wafers, reducing the volume of melt required for a growth run. The quartz cylinder and interior ampul walls were carbon coated to prevent melt adhesion in the region of the substrates.



- G26-0035-4, CdTe/GaAs/Si Substrate 2° off (100) ⇨ [111]



- CdTe/GaAs/Si Substrate 4° off (100) ⇨ [111]
- CdTe = 5.0 μm GaAs = .60 μm

Figure 18 *(a) XTEM of (111) CdTe on GaAs/Si Film using BF g = <220>; (b) cross-sectional TEM of {111} orientation CdTe film using BF g = <220> on GaAs/Si.*

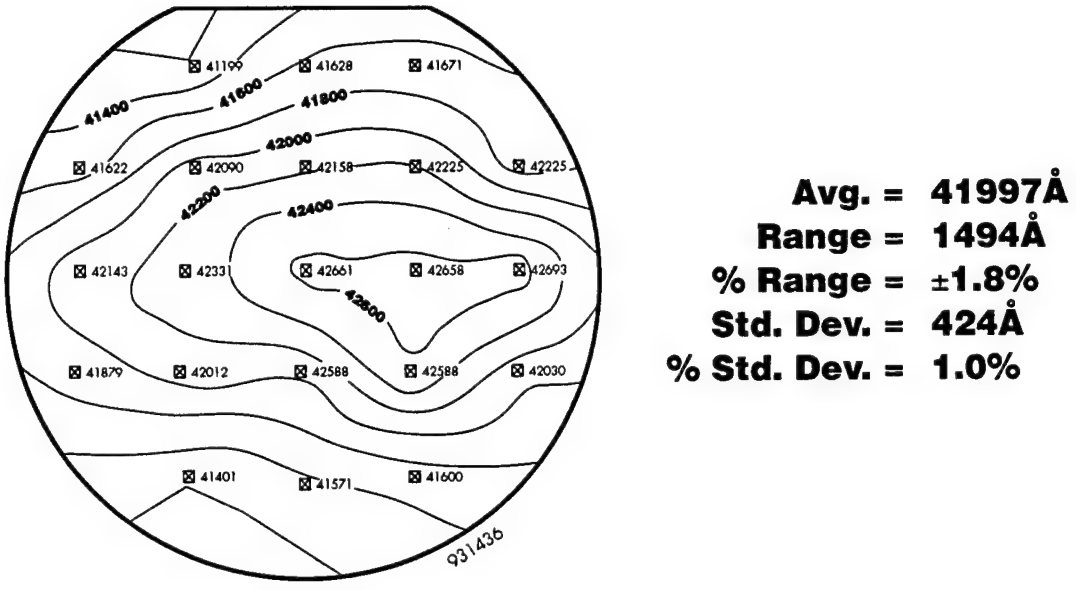


Figure 19 *Thickness uniformity mapping for $Cd_{0.96}Zn_{0.04}Te$ on 100 mm GaAs substrates deposited in Spire's SPI-MOCVD 3000G reactor.*

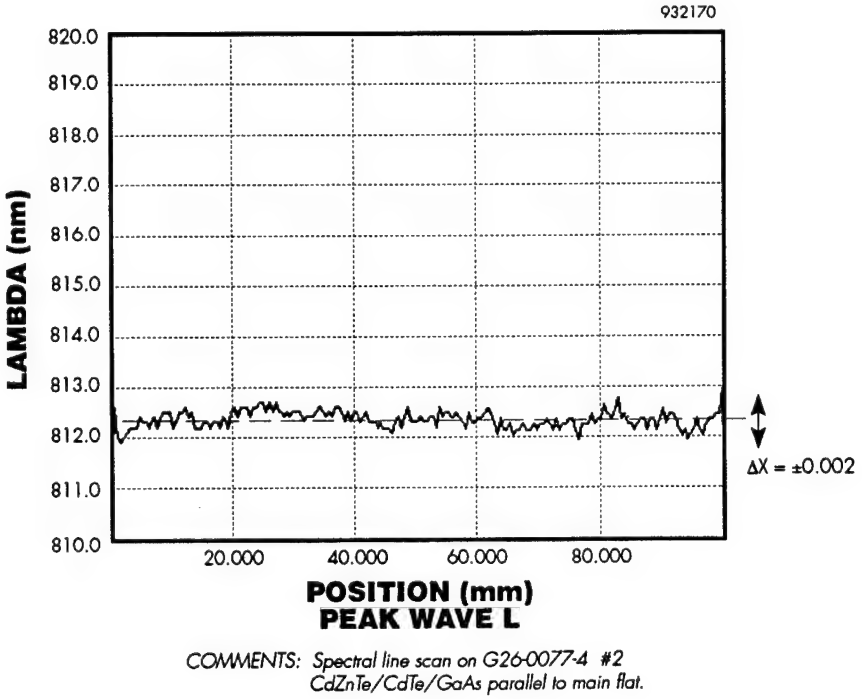


Figure 20 *Compositional uniformity across 100 mm CdZnTe/GaAs using high resolution photoluminescence mapping.*

All substrates used for these tipping growth experiments were Si wafers oriented about 4° away from (100) toward a [111] direction. They had a GaAs layer about 1 μm thick and a CdZnTe layer about 5 to 6 mm thick. The growth equipment utilized a tube furnace that could be tipped about a central axis, with the ampul placed in a uniform temperature zone close to the middle of the furnace. Control of the furnace temperature profile was the greatest difficulty encountered, because inverting the furnace resulted in a substantial change in the temperature profile as a result of the change in the heat transfer situation. A second heater winding, wound non-uniformly so as to supply heat preferentially to the furnace ends, was constructed and placed concentricity with the primary heater winding. This heater was controlled independently of the main furnace by a differential thermocouple in such a way as to drive the difference between the temperatures at the two ends of the ampul to zero. Unfortunately the response time of the furnace and control system was not short enough to prevent temperature excursions, that lasted throughout the 20 m growth time of the HgCdTe, when the furnace was tipped.

The growth process was carried out by heating the ampul to approximately 490°C, with the melt and source wafers at the lower end of the furnace. The temperature was held constant for 1 h so as to allow the melt to dissolve some CdTe from the source wafers and thus to become saturated with Cd. The temperature was then reduced by an amount that was varied from 5 to 10°C. Since the melt was still in contact with the source wafers it is expected that some of the CdTe dissolved in the melt was lost by deposition of HgCdTe onto the source wafer surfaces during this cooling phase, leading to a reduced degree of supersaturating. The furnace was then quickly inverted so that the melt covered the substrates. Growth was continued for 20 m, during which time the temperature was reduced by 5°C. After completion of growth the furnace was inverted slowly to decant the melt off the substrates. The furnace was allowed to cool to room temperature and the wafers removed.

Numerous difficulties were encountered with this growth method and only 6 growth runs were completed. Several runs were ruined because, on covering the substrates with the melt, the furnace controller reacted to the new thermal situation by applying sufficient heat to cause the furnace temperature to increase by 5°C or more, leading to dissolution of the CdZnTe and GaAs layers from the substrate and dissolution of some of the Si. In subsequent runs the power to the furnace was terminated immediately prior to tipping and was then controlled manually to produce the desired cooling rate.

When a temperature drop of 10°C was used, prior to immersing the substrates n the melt, a non-spectral HgCdTe film was formed on the substrate, with numerous droplets of melt being retained on the surface. Figure 21 is a Nomarski micrograph of the surface of a film of this type. The film appear to be covered with a large number of small crystallites, and it was concluded that excessive temperature drop after saturation of the melt had caused precipitation of HgCdTe crystallites. Films grown with only 5°C of initial supercooling were much smoother, Figure 22 is a micrograph of the film surface. The surface is rippled on a microscopic scale with occasional inclusions of melt in the surface. Figure 23 shows an FTIR transmittance spectrum of this film, the cut-on wavelength is approximately 3.1 μm and the thickness is about 8.3 μm. A sample of this film was cut and annealed at 250°C for 4 days in a saturated Hg atmosphere. After this anneal Hall measurements indicated the material to be n-type with a carrier concentration of 2.6E16/cm^3 and a mobility of 1.7E4 V.s/cm^2. The melt used was doped with In but this carrier concentration is a factor of 20 higher than would be expected for an uncontaminated film grown on a bulk substrate using this melt composition.

Figure 21 *Tipping growth - morphology (400X), supersaturation 10K.*

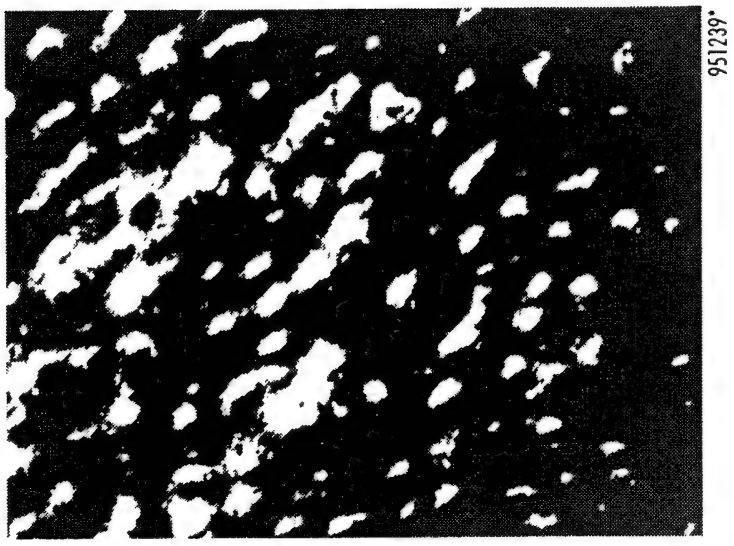


Figure 22 *Tipping growth - morphology (400X), supersaturation 5K.*

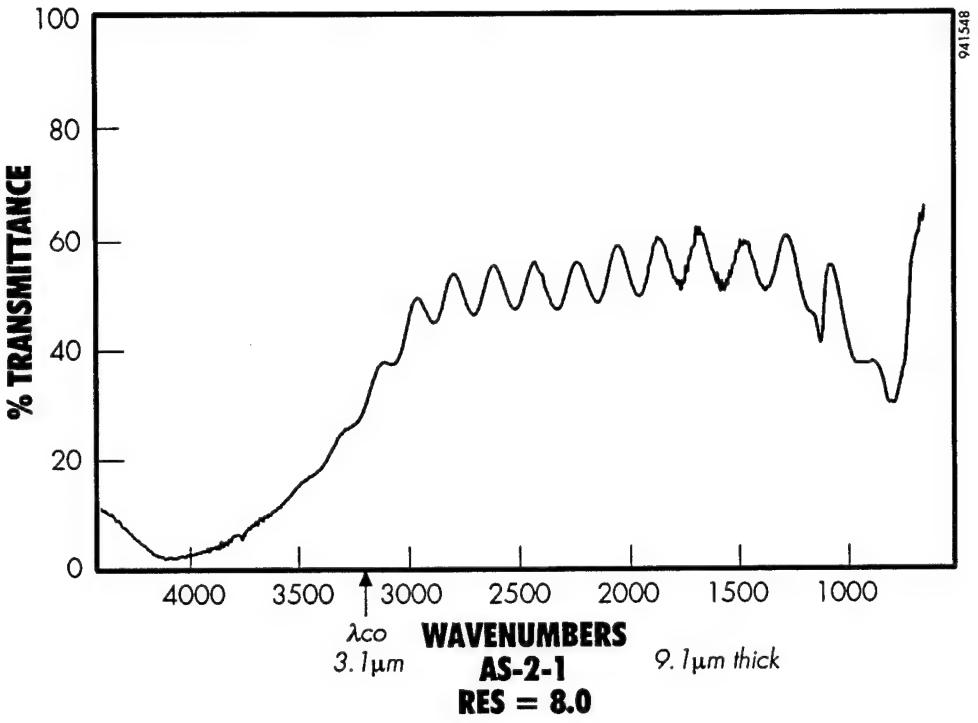


Figure 23 *FTIR transmittance spectrum.*

No failure of the thermal oxide encapsulant was observed during these experiments and so, since a reasonably low contamination level in the HgCdTe was observed, it was decided to abandon this growth method in favor of our well-established slider LPE technique. We continued with the use of 2 cm x 3 cm substrates since the LPE system used can accommodate two substrates of this size in a single growth experiment. This enabled us to use, for example, a Si-based substrate and a CdTe substrate next to each other in the same run.

Table 3 summarizes many of the results from the series of slider LPE base layer runs carried out on both Si-based and bulk CdTe substrates. Substrate numbers followed by an asterisk are CdTe. Run numbers ending in L or R refer to left and right substrates from the same growth run. The column "Sat. C" refers to the amount of supersaturation of the melt, in °C, at the start of growth. The SIMS data refers to the Ga concentration at a depth of about 4 μm into the film. The electron concentration "n" refers to the electron concentration measured after annealing the substrate at 250°C for 96h in a Hg-saturated atmosphere. The EPD given is the value obtained by using the Hahnert and Schenk etch (J. of Crystal Growth, Vol. 101, p. 251, 1990). All of the wafers used were on Si misoriented from (100) by 4° toward the [111] direction with the exception of the substrates for run AS006, for which the misorientation was 2° and 7° for substrates AS006R and L respectively.

The first run, AS001, resulted in meltback of the CdZnTe film from the substrate as a result of a temperature control malfunction. Si-based substrates in runs AS002 to AS005 had as-cut edges and showed melt attack at points along the edges and at the corners. The Hall data form these samples indicated a substantial amount of contamination of the melt. Electron concentrations approaching 1E18/cm^3 were measured except in run AS005, which had a low carrier

Table 3 *Results from the series of slider LPE base layer runs carried out on both Si-based and bulk CdTe substrates.*

LPE	Sustrt.	Date	Sat.	Gro.	Sat.	Thk.	Cuton	SIMS	n	Mobility	EPD	DC XR
Run #	Run #		C	C	C	mic.	mic.	cm-3	cm-3	cm^2/Vs	cm-2	arc s
AS001	104-2Z	7/21/93	3	2	485	0						
AS002L	6446-15	7/28/93	5	5	485							
AS002R	106-8C					46	8.3		5.5E+17	2.0E+.03	3.0E+06	86
AS003L	105-2Z	8/7/93	5	2.5	488	24	6.5		2.3E+17	4.0E+03	4.0E+06	
AS003R	106-7DC											216
AS004L	108-7AZ	8\26\93	3.5	2.5	488	20	6.4	2.0E+18	9.2E+17	6.8E+03	4.0E+06	
AS004R	108-7BZ											100
AS005L	108-8AZ	9/2/93	3	3	488	20	6.4		6.5E+13	2.2E+03	3.0E+06	216
AS005R	108-2BZ											
AS006L	108-6BZ	10/7/93	5	2.5	488	21	6.4				5.0E+06	
AS006R	108-5AZ										5.0E+06	
AS007L	106-2C	10/13/93	5	2.5	488	19	6.2					72
AS007R	108-4Z											90
AS008L	140-6Z	11/12/93	5	2.5	488	25	6.9	4.0E+17	1.4E+17	5.2E+03	8.5E+06	
AS008R	140-14Z											
AS009	B050113	12/7/93	5	2.5	488	21.5	6.7		1.5E+15	1.1E+05		
AS010L	159-2C	1/6/94	2	2.5	488	21.1	6	6.0E+16	2.4E+16	7.0E+04	1.5E+06	
AS010R	159-5C											
AS011L	159-3C	1/7/94	2	2	488	20.9	5.9					
AS011R	159-6C											
AS012L	166-8Z	1/10/94	2	2	488	20.5	5.9		1.5E+16	7.5E+04	1.2E+06	75
AS012R	162-2Z							1.5E+16				
AS013L	B0513311	1/14/93	2	2	488	13.1	6.4				4.8E+05	
AS013R	162-11Z											
AS014L	166-9Z	1/16/94	2	2	488	10.9	5.9					
AS014R	B0513311								2.4E+14	1.0E+05		
AS015	159-7C	1/28/94	2	2	488	15	5.9	3.0E+15	1.9E+15	7.2E+04	5.2E+05	
AS016	174-7Z	2/10/94	2	2	489	12.7	5.6					
AS017	159-4C	2/11/94	2	2	489	17.6	5.8					
AS018	174-6Z	2/14/94	2	2	489	17.8	5.7					

concentration but also a very low mobility and was evidently contaminated but closely compensated. SIMS analysis showed a Ga concentration that was about twice the electron concentration. The As concentration was much lower, as a result of the lower segregation coefficient for As incorporation from a Te-rich melt. The Ga concentration as a function of depth is shown in Figure 24. Runs AS006 and AS007 had mechanically rounded edges but were encapsulated with SiN. It was thought that adhesion of SiN to the substrate had been improved sufficiently to make it usable as an encapsulant, by use of an HF etch of the substrate surface before applying the SiN film. Unfortunately the SiN peeled almost completely off these substrates during the growth process, resulting in substantial attack of the substrate by the melt. It was not felt worthwhile to make Hall measurements on these films.

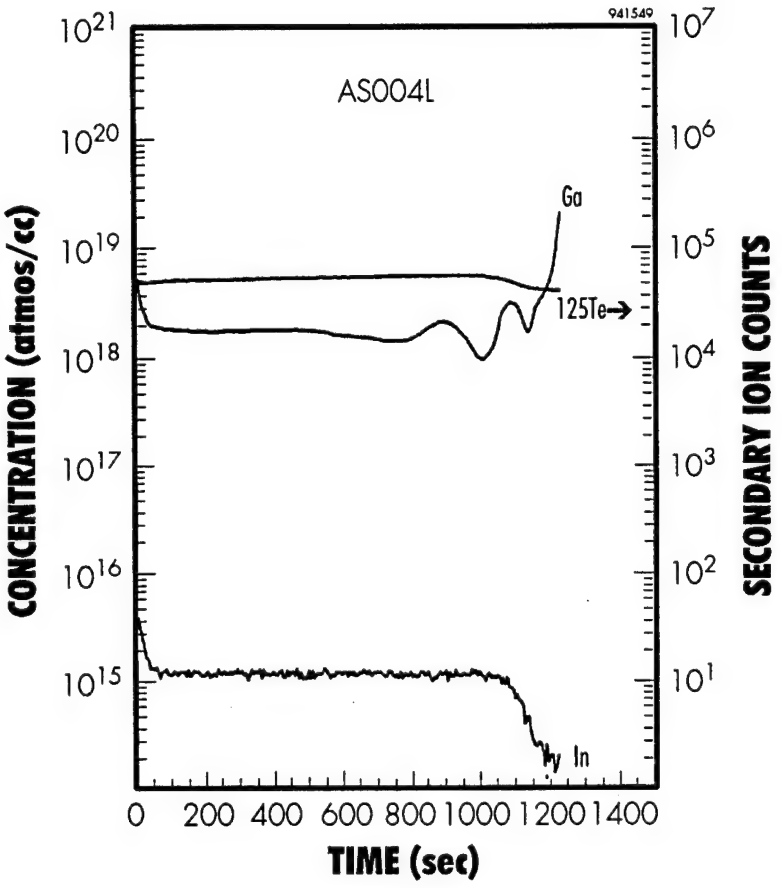


Figure 24 *Ga concentration as a function of depth.*

LPE run AS008 was made with a thermal oxide encapsulated substrate that had been mechanically edge rounded. Although no melt attack of the wafer edge could be seen, an electron concentration of 1.4E17/cm^3 was measured in this film. The Ga concentration obtained from SIMS analysis is shown as a function of depth in Figure 25. The presence of In is due to its deliberate incorporation in the melt. The measured Ga concentration at a depth of 4 μm is 4.0E17 atoms/cm^3 and decreases toward the interface with the substrate. This result indicated that an unknown source of Ga contamination was still active although no attack of the rounded substrate edge or peeling or apparent penetration of the thermal oxide encapsulant could be seen.

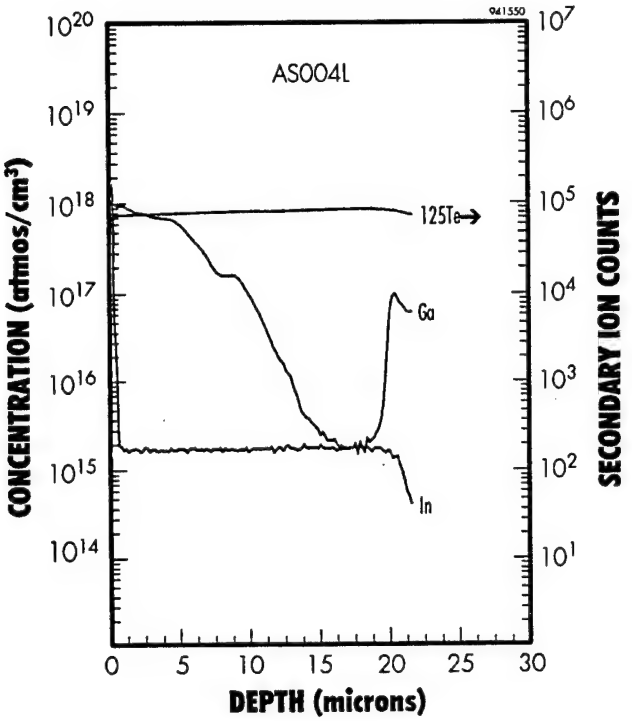


Figure 25 *Ga concentration obtained from SIMS analysis is shown as a function of depth.*

The SIMS profile is strong evidence that the source of contamination is not diffusion of Ga from the GaAs layer into the HgCdTe, since diffusion of Ga would result in a concentration that increased, not decreased, with depth, as the distance form the source of the Ga, i.e. the GaAs layer, decreased.

A possible source of Ga contamination was Ga remaining in the LPE system from earlier runs in which substantial melt contamination occurred. To evaluate this possibility, a run was made (AS009) using a conventional CdTe substrate only. Hall data indicated no contamination of the system, the measured electron concentration of 1.5E15/cm^3 and mobility of 1.1E5 cm^2/V.s for this run are the values to be expected from the In-doped melt used in a clean system.

The wafers from run AS008 were searched for locations where attack of the substrate may have occurred, resulting in melt contamination. After chipping some polycrystalline material away from the wafer edge, a region of substrate attack was seen just outside the perimeter of the LPE growth region. Further examination showed that this had also occurred in the earlier runs. The region of attack was in a line about 100 μm wide, just outside the growth area, where part of the CdZnTe film that was not covered by an encapsulant was also not contacted by the melt. The situation was as shown in Figure 26a, the encapsulant overlaps the front side of the substrate by 1 mm. The melt well is also about 1 mm smaller than the substrate so that any mis-registration of the melt allows the situation shown and the substrate is attacked. The mechanism for this attack is not well established, but it appears that the melt is under-saturated in a narrow region near the edge. This may be a result of loss of Hg by vaporization from this region. Reducing the Hg concentration in the LPE melt causes an increase in Cd solubility at a fixed temperature, i.e. the melt becomes under-saturated and will dissolve CdTe locally.

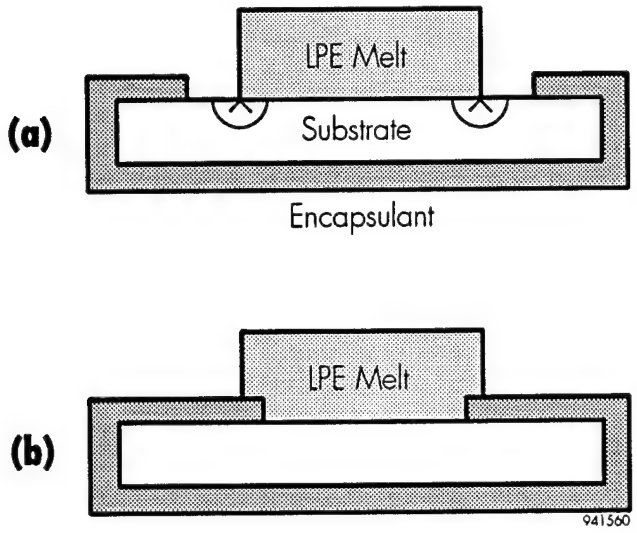


Figure 26 *Sources of substrate attack by melt.*

In order to avoid this problem, the width of the encapsulant border was increased so as to ensure that the periphery of the melt contacted an encapsulated part of the substrate, as shown in Figure 26b. Encapsulant border widths of 2 or 3 mm were tried. It was found in subsequent runs that even a 2 mm border was adequate to completely eliminate this problem. Run AS010 was made and showed an electron concentration of 2.4E16 with a Ga concentration, measured by SIMS, of 6.0E16 atoms/cm^3. Although this represented approximately a 10-fold reduction in donor contamination from run AS008, it is still too high a value for detector fabrication. A search was therefore made for the remaining sources of contamination.

Deposition of the GaAs layer on an encapsulated substrate results in a single crystal layer on the exposed Si window and some polycrystalline material on the oxide encapsulant frame. The GaAs growth rate is higher on the single crystal area but is still finite on the frame. It is well known from GaAs technology that the ratio of the growth rate on the oxide to that on the single crystal area increases with the width of the oxide area. There is therefore substantially more GaAs on a 3 mm wide encapsulant border as compared with a 2 mm wide one. When the CdZnTe is deposited, polycrystalline CdZnTe is deposited on the oxide at about the same rate that single crystalline material is deposited inside the window area so that the polycrystalline GaAs particles, which are typically in the form of small isolated spheres, are coated with polycrystalline CdZnTe.

Figure 27 is a micrograph of a typical area of the border of a substrate with a 2 mm border showing approximately spherical particles of GaAs overcoated with CdZnTe. During LPE growth part of this material is contacted by the melt and some of the polycrystalline GaAs is incorporated in the melt. Calculation shows that, if all of the polycrystalline GaAs were completely incorporated into the melt, a Ga concentration of 4E18/cm^3 would be incorporated into the HgCdTe, more than sufficient to explain the SIMS Ga concentration of 4E17 atoms/cm^3 and the electron concentration of 1.3E17/cm^3 actually measured for run AS008. By reducing the GaAs thickness from 1.0 μm to 0.5 μm and reducing the operating pressure, the amount of GaAs deposited on the encapsulant frame has been reduced, as shown in Figure 27, center picture.

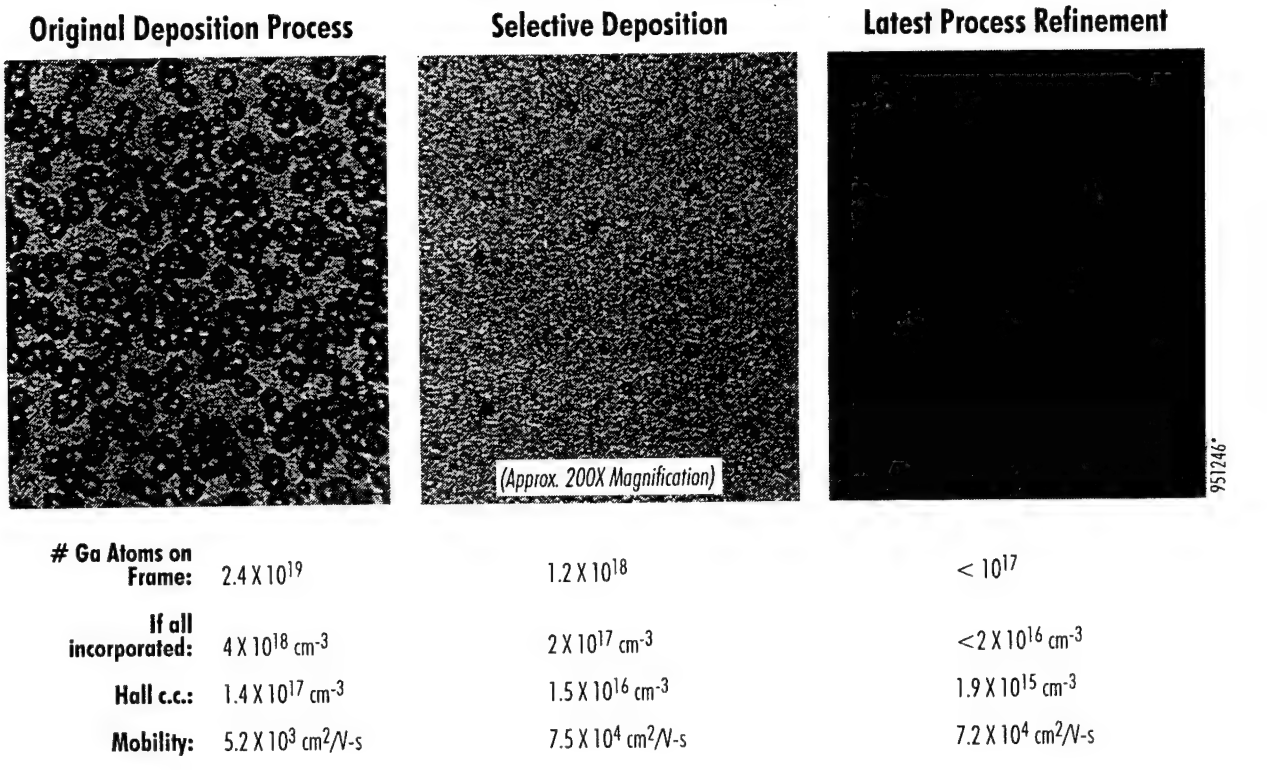


Figure 27 *MG-WC-1 LPE substrates (alternate) ploy-GaAs contamination reduced and tracks directly with LPE carrier concentration.*

Runs AS010, AS011, and AS012 were made with substrates having reduced GaAs deposition on the frame. The surface of run AS011 was inferior to that of the other two runs, indicating possible contamination in handling, and it was not processed further. The carrier concentration in the other two was 2.4 and 1.5E16/cm^3, the Ga concentration by SIMS was 6.0E16 atoms/cm^3. This represents a reduction in Ga by about an order of magnitude below the value for AS008.

A further reduction in GaAs depostion on the oxide encapsulant frame was made by using a new wafer carrier in the MOCVD system with recesses cut to the size and thickness of the wafers. Figure 27, the picture on the right, shows the very occasional specks of GaAs obtained by this process. A further reduction in contamination by approximately a factor of 2 would obviously result if only a single 2 cm x 3 cm substrate were placed in each growth run. The electron concentration obtained from run AS015, using only a single CdZnTe/GaAs/Si substrate, with the final improved GaAs deposition process, was 1.9E15/cm^3. SIMS analysis shows a Ga concentration of about 3.0E15 atoms/cm^3, decreasing to 3.0E14 atoms/cm^3 near the substrate interface, as shown in Figure 28. Run AS014 was made wit both a CdTe and CdZnTe/GaAs/Si substrate to determine the degree of melt contamination from a single Si-based substrate. An electron concentration of 2.4E14/cm^3 and mobility of 1E5 cm^2/V.s, was obtained on the CdTe substrate, indicating the absence of any appreciable contamination.

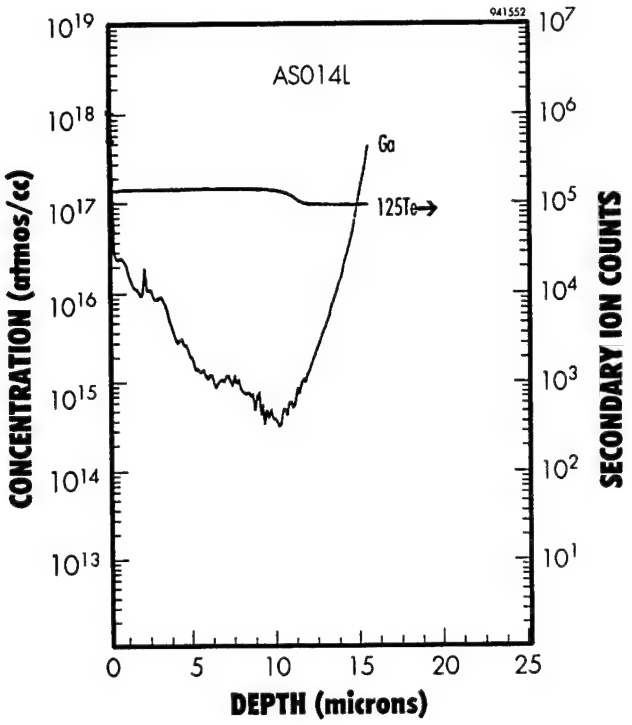


Figure 28 *SIMS analysis shows a Ga concentration of about 3.0E15 atoms/cm^3, decreasing to 3.0E14 atoms/cm^3 near the substrate interface.*

While carrying out these modifications to reduce the Ga contaminant level, the effect of degree of melt supersaturation at the beginning of growth was also varied. It was initially thought that this would have an effect on contamination level but this was not the case. A relationship between the degree of supersaturation and the dislocation density measured at the HgCdTe surface was noticed. Figure 29 shows the average dislocation etch pit density at the surface of the LPE base layer films as a function of the amount by which the melt temperature is reduced below the liquidus temperature before bringing it into contact with the substrate. As can be seen from this figure the dislocation density is reduced at lower amounts of supersaturation, presumably because the reduced initial growth rate and near-equilibrium growth conditions allow time for formation of a complete misfit dislocation network and reduction of the degree of disorder in subsequent growth.

After demonstrating a reduced contamination level, three runs, AS016, 017, and 018 were made and Hall samples cut from the ends of these samples. The first of these, Run AS016, showed poor surface morphology after cap growth, possibly because the Hg-rich melt had been changed immediately prior to growth on these Si-based substrates. Hall data on the p-on-n structure showed a very field-dependent Hall coefficient, as expected when a p-n junction is present. Unfortunately, after measurements had been made on the p-on-n structure, an error in the etch process used to remove the p-type layer resulted in the removal of both HgCdTe layers. The Hall measurement was then made on the remaining CdZnTe layers, and showed them to be n-type with carrier concentrations of 1E16 to 2E16/cm^3 and mobilities of approximately 5E3 cm^2/V.S. This Hall data confirms that the CdZnTe layer had not been appreciably contaminated with Ga, a donor in CdZnTe, during the growth or annealing of the HgCdTe overlayers.

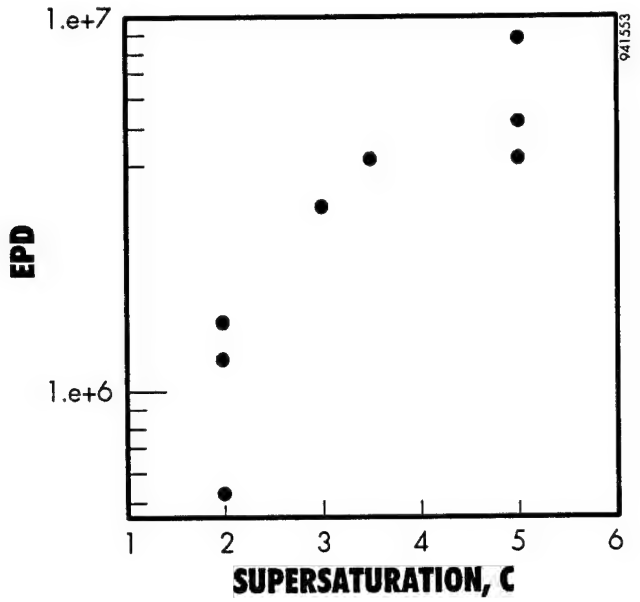


Figure 29 *The average dislocation etch pit density.*

The remaining parts of these wafers were used for photodiode fabrication. The decision was made not to simply make fast diode arrays from these wafers, but to use the A4 process and mask. This mask set gives both 64 x 64 arrays and numerous test diodes of various sizes. Use of the A4 mask set required substantial effort beyond what had originally been planned, especially in testing the arrays, and so was carried out under IR&D funds. The only variance from the standard A4 process was that ZnS passivation was used instead of CdTe in order to reduce process time. Cap layers of p-type HgCdTe were grown by dipping in an Hg-rich melt, an anneal in saturated Hg vapor at 250°C was used to convert the base layer to n-type, then mesa diodes were defined by wet chemical etching, the surface passivation layer of ZnS was deposited, metal contacts were deposited and defined, and the devices were tested.

2.7 Diode and Array Test Data

Figure 30 shows 80 K I/V curves for 60 μm x 60 μm mesas made on wafer AS017. RoA values are substantially below the expected range of 1000 to 5000 ohm.cm^2 for devices with an 8.6 μm cutoff, but the reverse characteristics are reasonably flat. Figure 31 shows a histogram of differential resistance at a bias of -20mV at 87K. The average value of 6.4E6 ohms is equivalent to RdA = 230 ohm cm^2. It is probable that higher reverse impedances would result from the use of CdTe passivation for future devices.

Figure 32 shows the photoresponse as a function of wavelength for these diodes at 80K, from which a cutoff wavelength of 8.6 μm is derived. Based on the fact that the quantum efficiency continues to increase at wavelengths appreciably below that of turn-on it is apparent that the base layer thickness is less than ideal and that the quantum efficiency could be improved somewhat by growing a thicker base layer although, as can be seen from Table 3, the base layers were determined by FTIR to be almost 18 μm thick for these devices. The peak quantum efficiency obtained was 48% with no correction for the fact that an estimated 30% of the incident radiation was reflected from the illuminated back side of the device, which consists of bare Si.

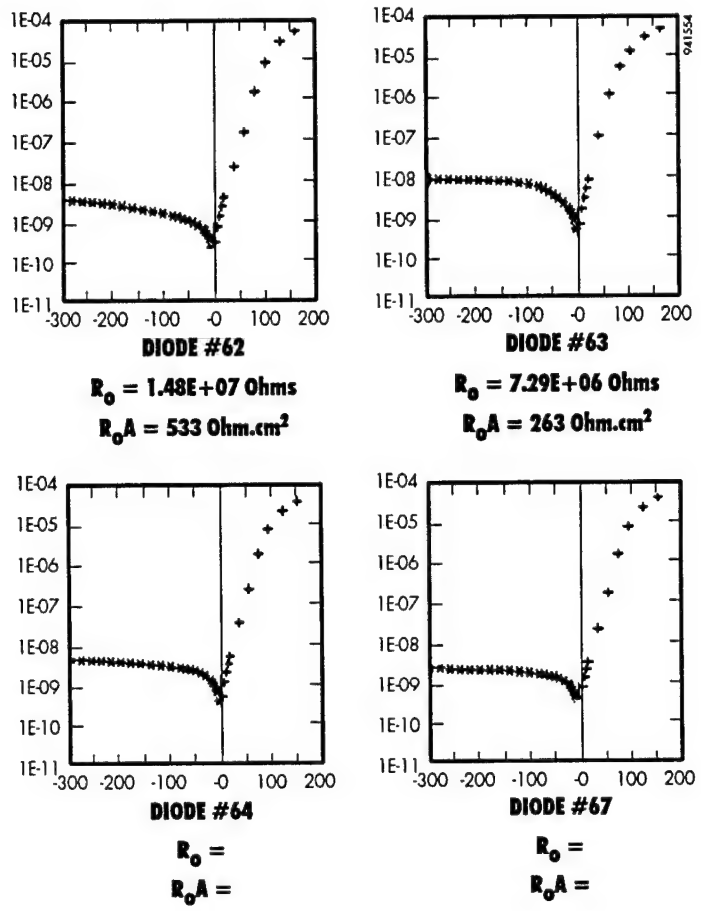


Figure 30 *80 K I/V curves for 60 μm x 60 μm mesas made on wafer AS017.*

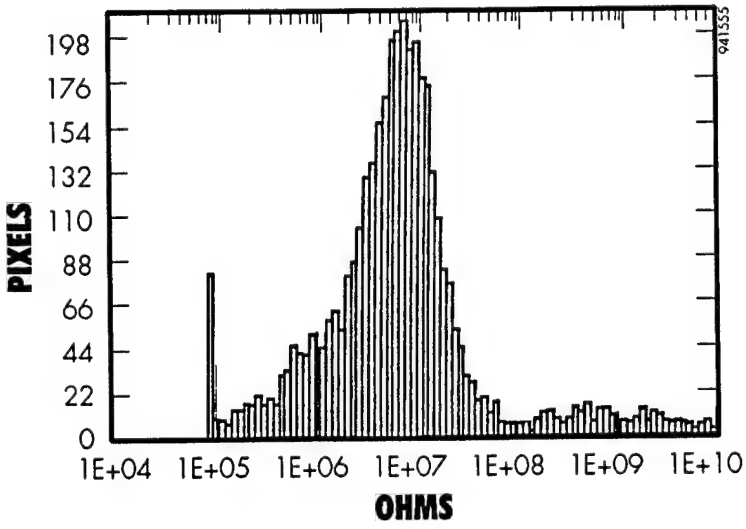


Figure 31 *A histogram of differential resistance at a bias of -20mV at 87K.*

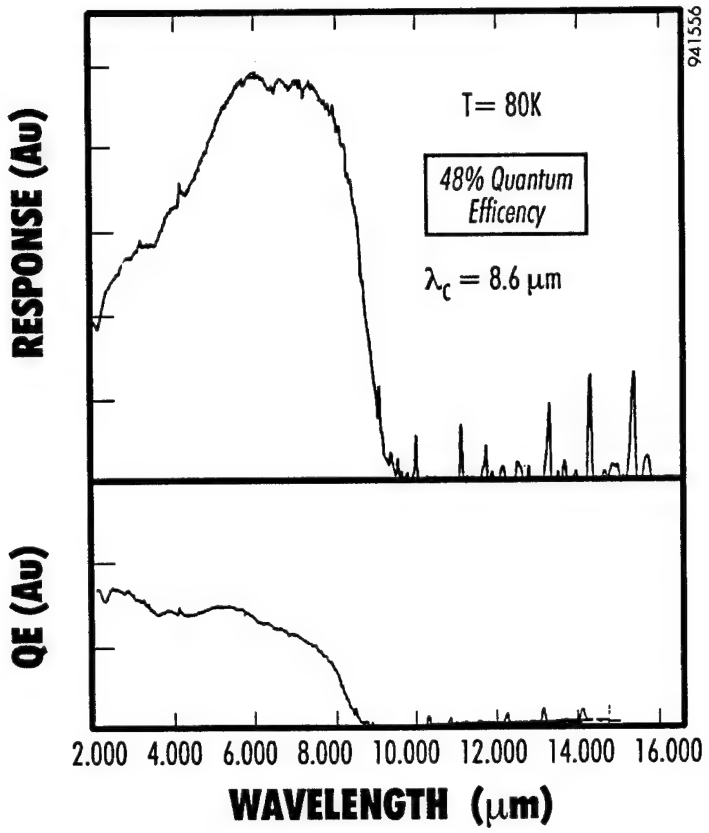


Figure 32 *The photoresponse as a function of wavelength for diodes at 80K, from which a cutoff wavelength of 8.6 μm is derived.*

Very similar results were obtained from wafer AS018, which also had a cutoff wavelength of 8.6 μm and a peak quantum efficiency of about 50%.

3 CONCLUSIONS

The substrate I program was successful in developing a number of essential processes and technologies necessary for successful production of CdZnTe/GaAs/Si substrates. As a result at the substrate I program a thermal oxide encapsulant has been developed that is impervious to the Te-rich LPE melt and is not wetted by it. This encapsulant has made it possible to reduce the Ga impurity level in LPE HgCdTe to below 1 x 10^{15} atoms/cm^3. Spire has installed a production scale MOCVD reactor SPI-MOCVD™ 3000G and a deposition process for large-area, CdZnTe/GaAs/Si substrates with excellent uniformity of thickness and composition. At the same time it has been found possible to produce CdZnTe deposits with a (111) B orientation that are free of twins at the surface and are of excellent crystalline quality with dislocation densities of down to 5 x 10^5/cm^2 and an X-ray rocking curve FWHM of below 80 arc.sec. Long-wave infrared diodes with a quantum efficiency of 50% (when illuminated through the uncoated Si substrate) have been produced form this material. Additional work is needed to optimize the thickness of the GaAs buffer layer, reduce the density of Ga speckles on the oxide mask, further reduce the defect density in the CdZnTe film, and implement real-time control of the CdZnTe composition for first pass success. I should add that elimination of the GaAs buffer by direct deposition of CdZnTe on Si may lead to high quality CdZnTe films while eliminating the risk LPE-melt contamination with Ga.

APPENDIX A

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Large Area Depositon of $Cd_{1-x}Zn_xTe$ on GaAs and Si Substrates by Metalorganic Chemical Vapor Deposition

N.H. KARAM, R. SUDHARSANAN, A. MASTROVITO, and M.M. SANFACON

Spire Corporation, One Patriots Park, Bedford, MA 01730

F.T.J. SMITH

Loral Infrared & Imaging Systems, Lexington, MA 02173

M. LEONARD and N.A. EL-MASRY

North Carolina State University, Raleigh, NC 27695

Results of large-area (up to 1000 cm^2/run) $Cd_{1-x}Zn_xTe$ heteroepitaxy on both GaAs and GaAs/Si substrates by metalorganic chemical vapor deposition (MOCVD) are presented. $Cd_{1-x}Zn_xTe$ (x = 0–0.1) films exhibited specular surface morphology, 1% thickness uniformity (standard deviation), and compositional uniformity (Δx) of ± 0.002 over 100 mm diam substrates. For selected substrate orientations and deposition conditions, the only planar defects exhibited by (111)B $Cd_{1-x}Zn_xTe$/GaAs/Si films were lamella twins parallel to the CdTe/GaAs interface; these do not propagate through either the $Cd_{1-x}Zn_xTe$ layer or subsequently deposited liquid phase epitaxy (LPE) HgCdTe layer(s). Background Ga and As-impurity levels for $Cd_{1-x}Zn_xTe$ on GaAs/Si substrates were below the secondary ion mass spectroscopy detection limit. Preliminary results of HgCdTe liquid phase epitaxy using a Te-rich melt on Si-based substrates resulted in x-ray rocking curve linewidths as narrow as 72 arc-sec and etch-pit densities in the range 1 to 3×10^6 cm^2.

Key words: CdZnTe/GaAs, CdZnTe/GaAs/Si, GaAs/Si, CdZnTe, heteroepitaxy, HgCdTe, liquid phase epitaxy (LPE), metalorganic chemical vapor deposition (MOCVD)

INTRODUCTION

The growth of heteroepitaxial $Cd_{1-x}Zn_xTe$ on sapphire, GaAs, and Si-based alternative substrates has attracted significant interest in recent years due to its potential for the fabrication of large-area HgCdTe infrared focal plane arrays (IRFPAs).[1–13] To date, the best IRFPAs are fabricated using liquid phase epitaxy (LPE) on bulk $Cd_{1-x}Zn_xTe$ substrates.[1,2] However, Si-based substrates have several advantages over these including availability in large diameters at lower cost, higher mechanical strength, thermal expansion match to Si-readout circuitry, and the prospect for monolithic integration of IRFPAs with Si-based integrated circuits (ICs). Successful deposition of $Cd_{1-x}Zn_xTe$ on GaAs and Si-based substrates has been demonstrated using metalorganic chemical vapor deposition (MOCVD),[7,8] hot wall epitaxy,[4] atomic layer epitaxy,[5,6] and molecular beam epitaxy (MBE).[9] The main hindrances to the progress of this alternative substrate technology are the high density of defects (5×10^6 to 1×10^7 cm^{-2}) resulting from the large lattice mismatch between CdZnTe and Si, and the thermal-expansion-coefficient mismatch which leaves the heteroepitaxial film under a residual bi-axial tensile stress. For this technology to reach its desired goals, large area $Cd_{1-x}Zn_xTe$ on Si-based substrates with defect densities lower by one to two orders of magnitude than have been achieved to date are required.

Although high defect density has been shown to degrade the low-temperature performance of IR-detectors, respectable high-temperature performance has been reported for IRFPAs fabricated using LPE-HgCdTe on MOCVD-$Cd_{1-x}Zn_xTe$/ GaAs/Si alternative

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substrates.[7,10] Heteroepitaxy of [111]B $Cd_{1-x}Zn_xTe$ on GaAs and Si-based substrates has been plagued with a high density of twins[12,13] which propagated into subsequently deposited LPE films, degrading their properties. This prompted researchers to develop LPE of HgCdTe on (100) $Cd_{1-x}Zn_xTe$ where twins are unstable. However, recent results for (111)B CdTe-on-sapphire showed that twin formation can be suppressed by proper selection of the deposition parameters, heat treatment, and wafer orientation.[14] In this paper, we report the first demonstration of large-area (18, 75 mm or ten, 100 mm wafers per run, a total area of 1000 cm^2) MOCVD of $Cd_{1-x}Zn_xTe$ on GaAs and GaAs/Si substrates resulting in excellent thickness and compositional uniformity. We also report initial results for LPE of HgCdTe on (111)B $Cd_{1-x}Zn_xTe$/GaAs/Si alternative substrates.

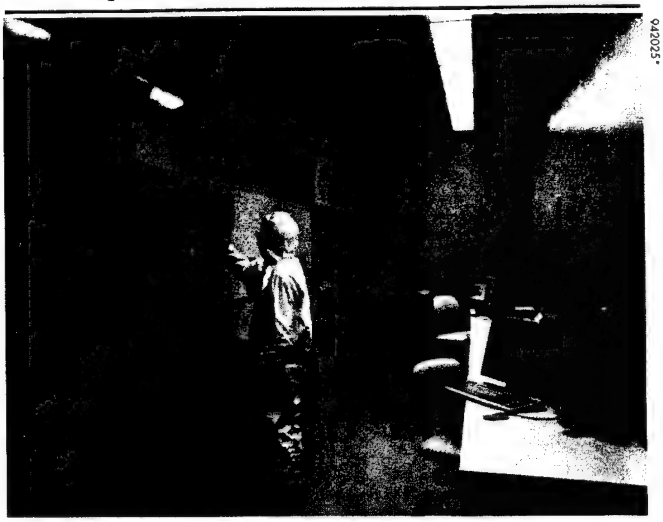

Fig. 1. Spire's dual-chamber production-scale SPI-MOCVDT™ 3000G reactor for III-V and II-VI compounds.

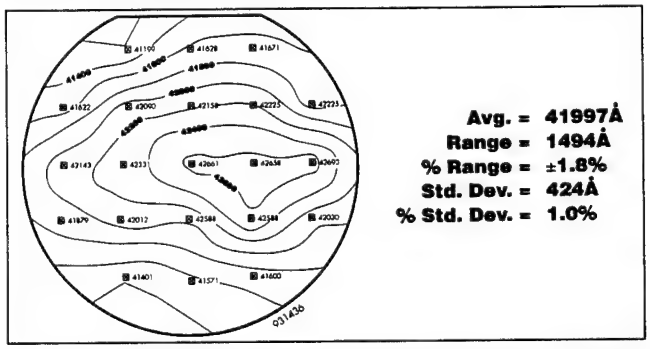

Fig. 2. Thickness uniformity contour map for (111) $Cd_{1-x}Zn_xTe$ deposited on a 100 mm GaAs wafers in SPI-MOCVD 3000G.

EXPERIMENTAL

Large-area MOCVD of (111) $Cd_{1-x}Zn_xTe$ has been achieved on (100) GaAs and (100) GaAs-on-Si substrates in a dual chamber, low-pressure MOCVD reactor, the SPI-MOCVD™ 3000G, which has a capacity of up to 18, 75 mm wafers or ten, 100 mm wafers per run. Figure 1 shows the dual-chamber reactor which is equipped with two independent gas handling systems for the separate deposition of III-V (e.g., GaAs) and II-VI compounds with no cross contamination. The GaAs-on-Si films were deposited using the conventional two-step process, reported earlier,[15] to thicknesses in the range of 0.5 to 2.5 μm. Dimethylcadmium (DMCd), dimethyltellurium (DMTe), and diethylzinc (DEZn) were used for Cd, Te, and Zn sources, respectively. In a typical deposition experiment for [111]B $Cd_{1-x}Zn_xTe$ on GaAs/Si, the substrate is first exposed to a short pre-growth bake to remove the native oxide and provide a Ga-rich surface. This is followed by a two-step deposition of CdZnTe at temperatures in the range 390 to 450°C, reactor pressures in the range 300 to 650 Torr, VI/II in the range 5 to 0.4, and a growth rate in the range 4 to 8Å/s.

The $Cd_{1-x}Zn_xTe$ films were characterized using Nomarski optical microscopy for surface morphology, optical reflectance spectroscopy (ORS)[16] for thickness measurement, and photoluminescence (PL) at 77K and room temperature for compositional measurement and uniformity. Secondary ion mass spectroscopy (SIMS) was used for impurity level determination. Double crystal x-ray diffraction (DXRD), Laué x-ray back reflection, cross-sectional transmission electron microscopy (XTEM), and selective-area electron diffraction (SAD) were used for structural characterization and determination of film orientation. Cross-sectional TEM samples were prepared using standard mechanical thinning followed by Ar^+-ion milling at 77K to achieve foil thicknesses in the range 0.2 to 0.5 μm. Samples were examined using a Hitachi-800 TEM operated at 200 kV acceleration voltage.

RESULTS AND DISCUSSION

Successful fabrication of $Cd_{1-x}Zn_xTe$ on Si-based alternative substrates requires addressing the following issues: thickness and compositional unifor-

Table I. Thickness Uniformity Data of $Cd_{1-x}Zn_xTe$ Films Grown on GaAs Substrates

Wafer No.	Size (Inches)	Average (Å)	Range (Å)	% Range	Standard Deviation	% Standard Deviation
G26-77-1	4	42472	1063	±1.3	330	0.8
G26-77-2	3	43358	1698	±2.0	433	1.0
G26-77-3	4	42914	1428	±1.7	443	1.0
G26-77-4	4	41997	1494	±1.8	424	1.0
G26-77-5	3	42547	978	±1.1	261	0.6
G26-77-6	4	42345	1432	±1.7	427	1.0

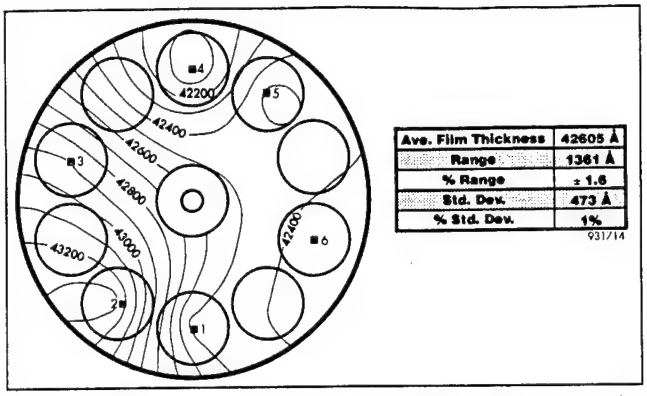

Fig. 3. Wafer-to-wafer thickness uniformity contour map for $Cd_{1-x}Zn_xTe$ films grown on GaAs substrates.

mity, background impurity level, surface morphology, film orientation, and defect density. In this paper, we discuss these issues with specific emphasis on the (111)B orientation of $Cd_{1-x}Zn_xTe$.

Thickness and Compositional Uniformity of $Cd_{1-x}Zn_xTe$

The thickness and compositional uniformity of $Cd_{1-x}Zn_xTe$ films grown in Spire's production-scale, SPI-MOCVD 3000G reactor were measured on 75 and 100 mm diam GaAs wafers oriented 2° off (100) → [110]. The GaAs wafers were positioned in such a way that uniformity across the entire susceptor could be mapped. Thickness uniformity mapping used ORS, a nondestructive tool that can reliably measure $Cd_{1-x}Zn_xTe$/GaAs film thickness with an accuracy of ±5 nm. Thirteen-point and 21-point thickness measurement mapping was performed on 75 and 100 mm wafers, respectively. Figure 2 shows the thickness uniformity of a $Cd_{1-x}Zn_xTe$ film on a 100 mm GaAs substrate. Table I shows thickness uniformity data for all the wafers in a six-wafer growth lot which yielded 1% standard deviation (see Fig. 3).

The composition of $Cd_{1-x}Zn_xTe$ films was routinely estimated using 77K PL,[10] and was found to be in good agreement with DXRD measurements. Room temperature PL mapping was used to determine compositional uniformity of $Cd_{1-x}Zn_xTe$ films grown on 100 mm GaAs substrates. These measurements were done at the SCANTEK company in France. Line-scan peak-wavelength measurements were performed at 42 points across the 100 mm wafer and composition variation across the wafer was determined by converting the peak wavelength to $Cd_{1-x}Zn_xTe$ composition.[11] Figure 4 shows typical variation of the peak wavelength across a 100 mm $Cd_{1-x}Zn_xTe$/GaAs wafer. Using data from Fig. 4 and the calibration given in Ref. 11, the average composition is 0.027 and ±0.002, respectively.

Impurity Level

Ga and As impurity levels in CdZnTe films on GaAs and GaAs/Si substrates have been measured by SIMS. The measurements employed an O_2+ beam with a net impact energy of 8 keV and a sputter rate of 9 nm/s.

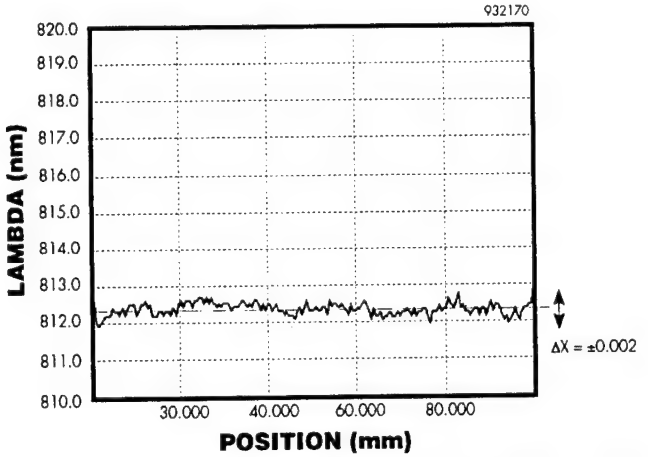

Fig. 4. Compositional uniformity mapping across 100 mm $Cd_{1-x}Zn_xTe$/GaAs using high resolution photoluminescence.

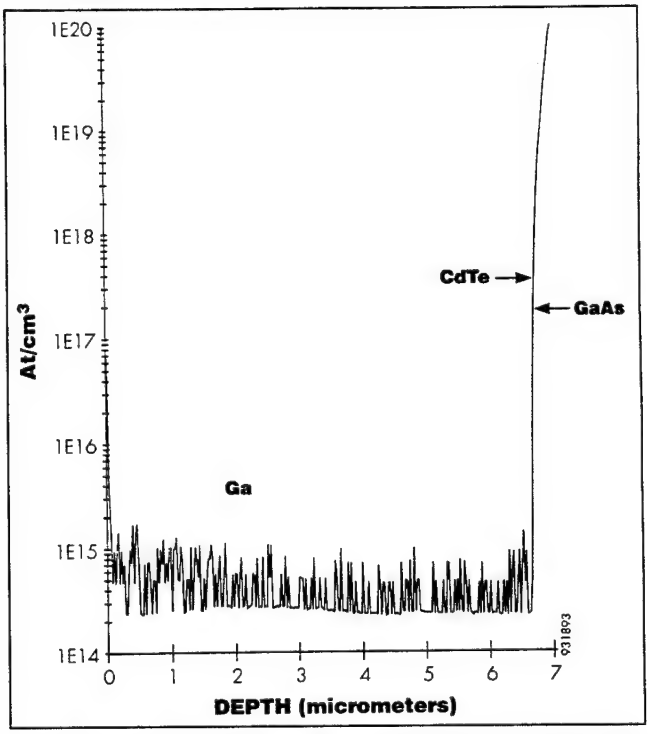

Fig. 5. Secondary ion mass spectroscopy profile for Ga impurity level in CdTe/GaAs/Si structure.

Figure 5 shows the Ga concentration as a function of film depth for a 6.5 μm thick CdTe/GaAs/Si film. The average Ga concentration was 5×10^{14} cm^{-3}, which is approximately the SIMS detection limit. No arsenic was detected in these films (the As detection limit is approximately 3×10^{16} cm^{-3}). These results indicate that Ga and As diffusion at our baseline growth conditions is very limited. We have not observed a significant difference in impurity levels between CdTe and $Cd_{1-x}Zn_xTe$ films on GaAs coated Si substrates. However, the Ga impurity level in CdTe on GaAs substrates is an order of magnitude higher, which could be due to autodoping from the GaAs wafer.

Surface Morphology and Film Orientation

To achieve (111)B $Cd_{1-x}Zn_xTe$ films with the im-

proved surface morphology and reduced defect density that are needed for LPE of HgCdTe, we have investigated a number of Si and GaAs wafer orientations and deposition conditions. The GaAs wafer orientations investigated were exact (100) and 2° off (100) toward the [110], while the Si wafer orientations investigated were 0, 2, 4, 7, and 10° off (100) toward the [111]. For the initial screening experiments, 1 μm thick GaAs-on-Si films with typical x-ray rocking curve FWHM in the range 200 to 400 arc-sec and surface roughness of ±30 nm were used. The deposition parameters for optimal compositional and thickness uniformity of $Cd_{1-x}Zn_xTe$ (x = 0.04) on GaAs were initially used, although the VI/II ratio had to be optimized for each orientation to achieve specular surface morphology. Figure 6 shows typical surface morphology for 5–10 μm thick films grown on GaAs and GaAs/Si substrates of various orientations. In general, all films exhibited specular mirror-like surface morphology. Films deposited on substrates with low off-axis misorientation (<2°) had smoother surfaces, while those deposited on substrates with higher off-axis misorientation (up to 10°) had regular fine features that were stable as a function of film thickness.

The orientation of the heteroepitaxial $Cd_{1-x}Zn_xTe$ films was determined using Laué x-ray back reflection measurements and confirmed by SAD patterns on XTEM samples. The accuracy of Laué x-ray back reflection measurements is ±0.5°. The dependence of $Cd_{1-x}Zn_xTe$ film orientation on that of the starting substrate is summarized in Table II.

For wafers misoriented off the (100) Si toward the [111] Si pole, $Cd_{1-x}Zn_xTe$ films were found to be misoriented off the CdTe (111)B direction toward the same [111] Si pole. The degree of misorientation of the $Cd_{1-x}Zn_xTe$ film off the (111) $Cd_{1-x}Zn_xTe$ direction was greater than that of the Si substrate surface normal off the (100) Si direction. Moreover, CdTe films deposited on direct (100) GaAs had an exact (111) orientation. Finally, $Cd_{1-x}Zn_xTe$ films deposited on 2° off (100) toward [110] GaAs were misoriented by the same degree off the (111)B $Cd_{1-x}Zn_xTe$ toward the [110] GaAs.

Cross-sectional TEM was used to investigate the effect of substrate misorientation on defect formation and twin propagation. By adjusting growth conditions, similar defect features have been observed in $Cd_{1-x}Zn_xTe$ films deposited on Si substrates oriented 2, 4, and 7° off (100) toward the [111]. Figure 7 shows a typical XTEM bright field image (g = 220) for CdTe/GaAs/Si 2° off (100) toward [111]. These measurements clearly indicate that thin lamella twins exist parallel to the CdTe/GaAs interface. The twins form

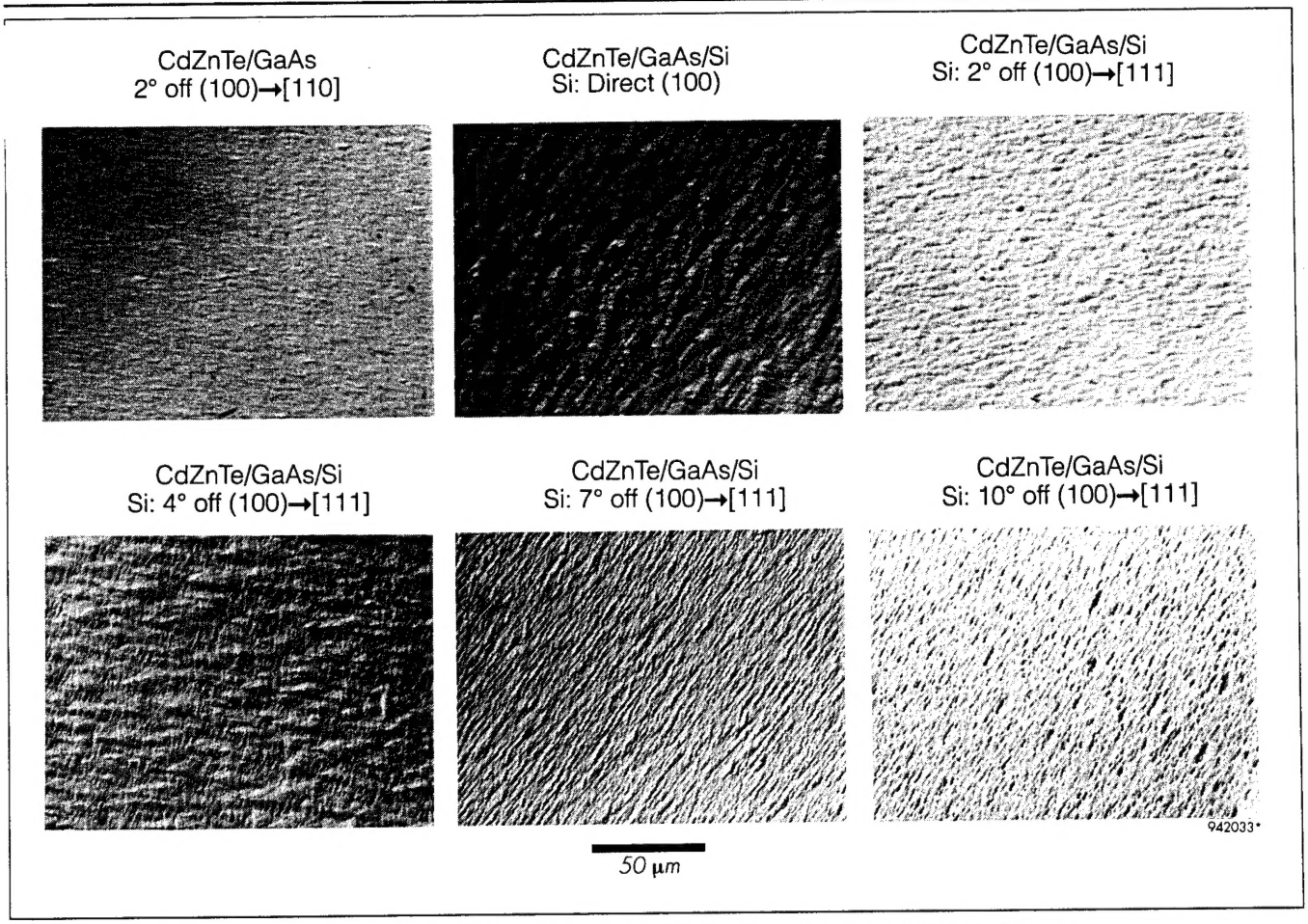

Fig. 6. Surface morphology of $Cd_{1-x}Zn_xTe$ films deposited on GaAs and GaAs/Si substrates with different orientations.

Table II. Dependence of $Cd_{1-x}Zn_xTe$ Film Orientation on GaAs and GaAs/Si Substrate Misorientation

Sample No.	Structure	Substrate Orientation (Laué)	$Cd_{1-x}Zn_xTe$ Film Orientation
G26-0035-4	CdTe/GaAs/Si	(100) off 2° → [111]	(111) off 3° → [111]Si
G26-0027-2	CdTe/GaAs/Si	(100) off 4° → [111]	(111) off 5° → [111]Si
G26-0035-2	CdTe/GaAs/Si	(100) off 7° → [111]	(111) off 9° → [111]Si
G26-0091-5	CdTe/GaAs/Si	(100) off 10° → [111]	(111) off 12° → [111]Si
G26-0006-1	CdTe/GaAs	exact (100)	exact (111)
G26-0013-1	CdTe/GaAs	(100) off 2° → [110]	(111) off 2° → [110]Si
C26-0064-2	$Cd_{1-x}Zn_xTe$/GaAs	(100) off 2° → [110]	(111) off 2° → [110]Si

in the early stages of growth and are confined near the CdTe/GaAs interface. Further, these twins seem to block the propagation of threading dislocations into the epitaxial layer. Figure 8 shows an XTEM for CdTe/GaAs/Si 4° off (100) toward [111]; the inset electron diffraction (SAD) pattern close to the CdTe/GaAs interface shows the extra diffraction spots due to the presence of twins near the interface, while the SAD pattern near the surface shows that the film is twin-free. Further deposition and characterization by etch-pit measurements of the HgCdTe films by LPE on these substrates showed that the twins do not propagate into the HgCdTe film.

Figure 9 is a XTEM bright field image (g = 220) of (111)B $Cd_{1-x}Zn_xTe$ (x = 0.03)/CdTe/GaAs (100) off 2° → [110]. This orientation is of special interest since no twinning has been observed by TEM. The same deposition conditions were used to grow 6.7 μm thick $Cd_{1-x}Zn_xTe$ on 100 mm GaAs of the same orientation (sample G26-0088, Table III). X-ray analysis on this wafer by Rockwell[14] indicated that twinning is below the detection limit (<1%). Another interesting feature of Fig. 9 is the bending of dislocations at the $Cd_{1-x}Zn_xTe$/CdTe interface, suggesting that a $Cd_{1-x}Zn_xTe$ strained layer can effectively reduce the dislocation density in the film.

LPE of HgCdTe/$Cd_{1-x}Zn_xTe$/GaAs/Si

Preliminary results of HgCdTe deposition on (111)B CdZnTe/GaAs/Si substrates using Te-rich LPE slider are very promising. Figure 10 compares the surface morphologies of GaAs/Si, $Cd_{1-x}Zn_xTe$/GaAs/Si, and LPE HgCdTe/CdTe/ GaAs/Si. The morphology of the GaAs/Si film is typical for a 1 μm film, corresponding to a surface roughness of approximately ±30 nm. In comparison, typical surface roughnesses for CdTe (6 μm thick), $Cd_{1-x}Zn_xTe$ (6 μm thick), and HgCdTe (20 μm thick) films on these GaAs/Si substrates are 65, 60, and 900 nm, respectively. The HgCdTe film (AS002R) is approximately 46 μm thick, as measured by FTIR, and is characterized by a wavy, cross-hatched surface.

Table III shows the x-ray rocking curve characteristics, film thickness, and cut-on wavelength for HgCdTe deposited on both CdTe/GaAs/Si and $Cd_{1-x}Zn_xTe$/GaAs/Si substrates. All of the HgCdTe results reported here are on (111) CdZnTe on GaAs on Si (100) off 4° → [111]. Defect densities in the LPE HgCdTe films have been measured, using the recently reported etchant by I. Hahnert and M. Schenk,[17] and found to be in the range 1 to 3×10^6 cm^{-2}. Latest results indicate that specular HgCdTe surface morphologies are achievable for selected Si-wafer orientations and $Cd_{1-x}Zn_xTe$/GaAs/Si growth conditions.

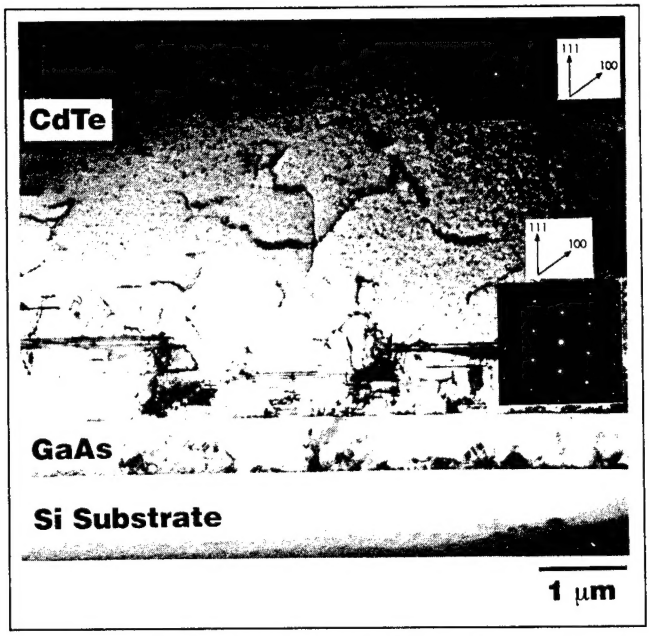

Fig. 7. Cross-sectional TEM of (111) oriented CdTe films on GaAs/Si substrate with (100) off 2° →[111] misorientation.

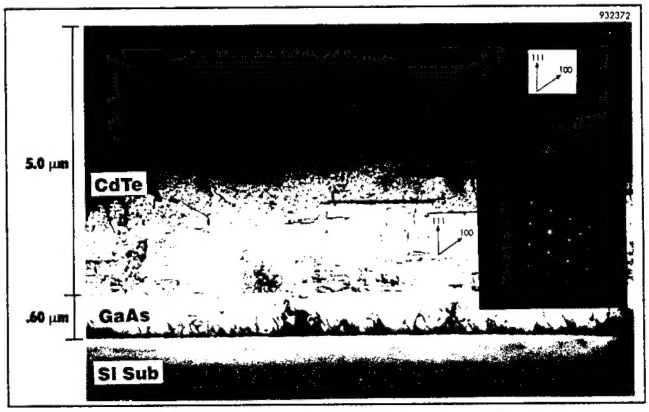

Fig. 8. Cross-sectional TEM of (111) oriented CdTe films on GaAs/Si substrate with (100) off 4° → [111] misorientation. Insets show selected area electron diffraction (SAD) pattern taken near CdTe/GaAs interface and at CdTe film.

Effects of misorientation off the (111)B axis on surface morphology, crystalline perfection, and electrical properties of LPE-HgCdTe films are currently under investigation. The narrowest x-ray rocking curve FWHM achieved to date is 72 arc-sec for sample AS007R, a 19.5 μm HgCdTe film (cut-on wavelength of 6.5 μm), deposited on CdTe/GaAs/Si.

Fig. 9. Cross-sectional TEM of (111) oriented CdTe films on GaAs substrate with misorientation (100) off 2° → [110] showing no twins.

CONCLUSIONS

We have demonstrated large-area uniform MOCVD of $Cd_{1-x}Zn_xTe$ with excellent thickness and compositional uniformity in a production scale SPI-MOCVD 3000G reactor. It has further been shown that (111)B $Cd_{1-x}Zn_xTe$/GaAs/Si alternative substrates are suitable for LPE, MOCVD, or MBE deposition of HgCdTe. Specular morphology of CdZnTe films on GaAs and GaAs-on-Si substrates has been achieved. For optimized deposition conditions, thickness uniformity in the range 0.6 to 0.8% is typical for growths on multiple three and four inch diameter wafers per run. A 1% standard deviation wafer-to-wafer thickness uniformity is obtained for $Cd_{1-x}Zn_xTe$/GaAs (x = 0.04) over the entire susceptor. Typical composition uniformity of $\Delta x = \pm 0.002$ across a 100 mm substrate has been achieved for $Cd_{1-x}Zn_xTe$ in the production scale reactor. Secondary ion mass spectroscopy shows that Ga and As impurities are below the detection limit (5×10^{14} cm^{-3}) in films deposited on GaAs-on-Si substrates. For selected wafer orientations and deposition conditions, transmission electron microscopy

Table III. Typical X-Ray FWHM for CdZnTe and HgCdTe of Different Thicknesses

Wafer ID No.	Structure	CdZnTe MOCVD Growth Temp (°C)	Cut-On λ (μm)	Thickness (μm)	X-Ray FWHM (arc-sec)
G26-073-1	CdTe/GaAs	420	—	3.0	144
G26-0120-8	CdTe/GaAs/Si	420	—	4.9	144
AS002R	HgCdTe/CdTe/GaAs/Si	—	8.3	46	86
AS007R	HgCdTe/CdTe/GaAs/Si	—	6.5	19.5	72
G26-088-7	$Cd_{1-x}Zn_xTe$/GaAs	420	—	6.7	135
G26-0121-7	$Cd_{1-x}Zn_xTe$/GaAs/Si	420	—	9.5	237
AS004R	HgCdTe/ $Cd_{1-x}Zn_xTe$/GaAs/Si	—	6.7	20	100

Note: GaAs wafer orientation: 2° off (100) toward [110]; Si wafer orientation: 4° off (100) toward [111].

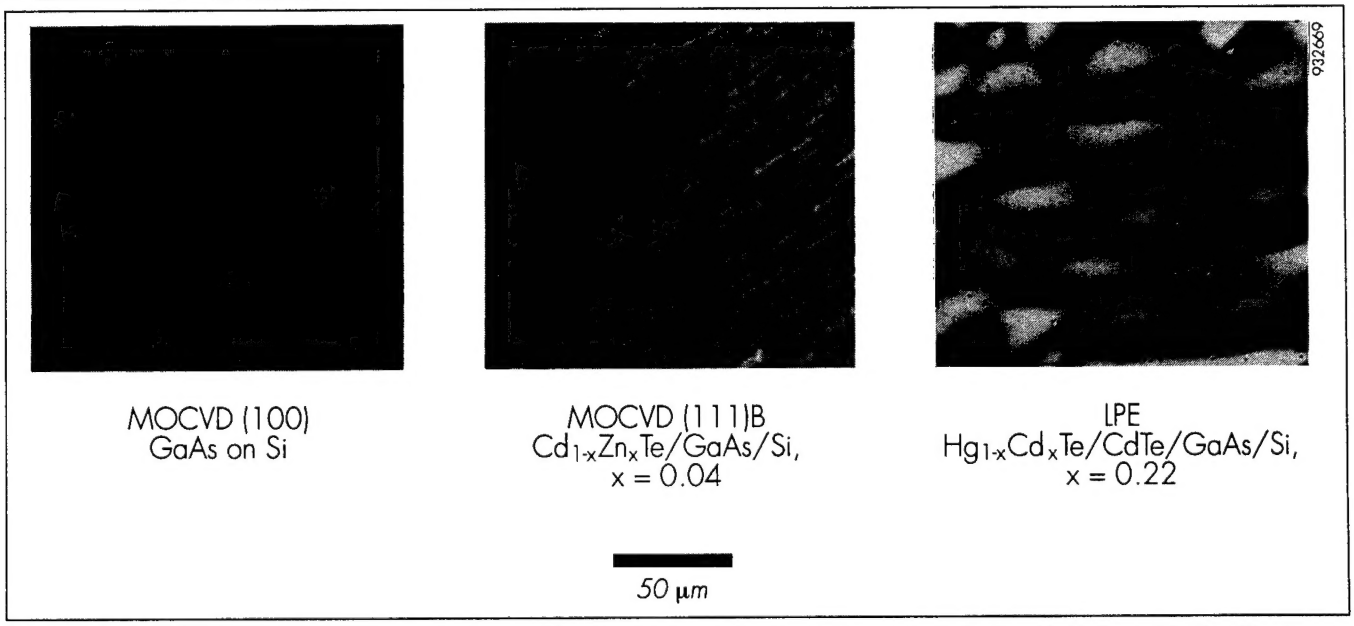

Fig. 10. A comparison of the surface morphology for GaAs on Si, $Cd_{1-x}Zn_xTe$/GaAs/Si and HgCdTe/$Cd_{1-x}Zn_xTe$/GaAsISi. The Si-substrate orientation is (100) off 4° → [111].

shows that only lamella twins parallel to the CdTe/GaAs interface form, while inclined twins are suppressed. The lamella twins do not propagate through subsequently deposited LPE HgCdTe layer(s). The surface morphology of these films is comparable to LPE HgCdTe films deposited on bulk $Cd_{1-x}Zn_xTe$ substrates. Etch-pit density measured for as-deposited Te-rich LPE-HgCdTe films on [111]B $Cd_{1-x}Zn_xTe$/GaAs/Si is typically in the range 1 to 3×10^6 cm^{-2}. Metalorganic chemical vapor deposition of $Cd_{1-x}Zn_xTe$ on GaAs on Si promises low-cost production of alternative substrates to the IRFPA community.

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